Towards Real-Time Implementation of Coherent Optical Communication

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Abstract: We outline the hardware architecture of coherent optical receivers supporting >40 Gb/s data rates and extract constraints for compatible signal processing algorithms. Additionally a chipset layout for a 40 Gb/s digital coherent polarization-multiplexed QPSK receiver is presented.

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1. Introduction

Advanced modulation formats such as quadrature phase shift keying (QPSK), multi-level quadrature amplitude modulation (QAM) and orthogonal frequency division multiplexing (OFDM) in combination with polarization-multiplex, coherent detection and digital signal processing are the most promising solutions for optical transmission systems with 100 Gb/s data rate or above. They offer a high spectral efficiency and high tolerance against chromatic dispersion (CD) and polarization-mode dispersion (PMD). The compensation of fiber impairments in the electronic digital domain additionally allows the application of powerful algorithms. The phase and frequency offsets between signal and local oscillator laser can be tracked, even if DFB lasers are employed [1]. Polarization crosstalk, CD and PMD can be compensated and also nonlinear phase noise can be mitigated [2]. Several real-time experiments using such algorithms have already been demonstrated [3,4]. But due to the high complexity in the implementation of real-time coherent receivers, offline digital signal processing is used in most experiments [5,6]. It is a very useful way to investigate new algorithms without the need to do extensive hardware development. However, careful consideration of the constraints for real-time applicability is necessary for the applied algorithms to ensure the usability in real systems.

In order to support this process in this paper we describe the general hardware architecture for digital signal processing in real-time coherent receivers and extract fundamental constraints for compatible algorithms. Additionally we present the layout of a mixed-signal/digital chipset for a 40 Gb/s realtime coherent receiver for polarization-multiplexed QPSK modulated signals.

2. Constraints for real-time coherent receiver algorithms

The high data rates in optical communication of 43 Gb/s, 112 Gb/s or even above generate stringent constraints for the algorithms suitable for real-time coherent receivers (Fig. 1). The receiver consists of an optical frontend including optical 90° hybrids, O/E conversion, analog-to-digital converters (ADCs) and a digital signal processing unit (DSPU). ADCs and DSPU can either be integrated in a single chip to ease interfacing and reduce the footprint [4], or in a modular approach for optimized performance, where ADCs and DSPU can be developed in different technologies for maximum bandwidth and high integration, respectively [7].

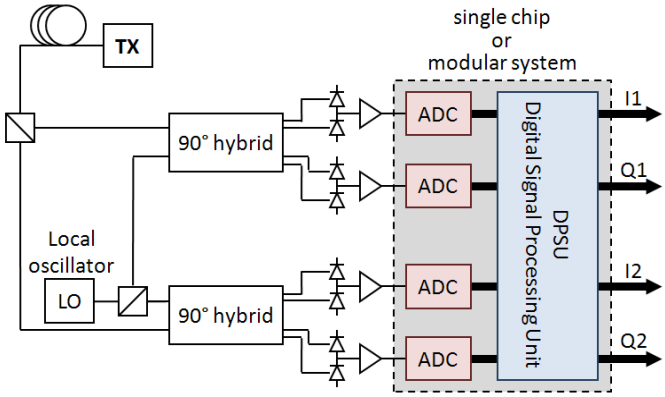

Fig. 1. Coherent optical receiver structure

In both topologies the implemented algorithms must allow parallel processing as shown in Fig. 2. The DSPU cannot operate directly at the sampling clock frequency of the analog-to-digital converter, which is in general 10 GHz or higher, but requires demultiplexing to process the data in m parallel modules at clock frequencies below 1 GHz. This allows automated generation of the layout, which is indispensable due to the complexity of the system. A comparison between the sampling clock frequency and the divided clock shows that at least $m \geq 16$ parallel modules are required. Algorithms for real-time applications should therefore theoretically allow parallel processing with an unlimited number of demultiplexed channels. The requirement for this is that the output of one module is independent of the outputs of the other parallel modules. A good example is the comparison of two filter structures: Finite impulse response (FIR) filters and infinite impulse response (IIR) filters. Fig. 3 depicts both structures in both serial and parallel systems. It can be seen that it is easily possible to parallelize an FIR filter. Though neighbouring modules depend partly on the same inputs, but they do not depend on the output signal of another parallel module. In contrast it is impossible to realize in practice the parallel structure shown for the IIR filter, because the output of the each module depends on the outputs of all previous parallel modules. An extremely low clock frequency would be needed to allow all calculations to be executed within one clock cycle. This would result in an even higher number of parallel modules, which makes an implementation unfeasible.

Another constraint for real-time coherent receiver algorithms is hardware efficiency, which also originates from the parallel processing in the DSPU. Because most of the required algorithm blocks have to be implemented m times within the DSPU, computationally intensive algorithms require a huge amount of chip area and therefore increase power consumption and cost. The implemented algorithms should therefore not only be evaluated by performance, but also by hardware efficiency. One way to increase hardware efficiency is to use signal transformations, e.g. FFT/IFFT, log-function or transformation to polar coordinates ($x = r\cos\varphi$, $y = r\sin\varphi$). Although the transformation itself requires additional hardware effort, this is often beneficial because of the simplifications in subsequent calculations. For example an FFT can reduce a convolution to multiplications, or the log-function or polar coordinates allow to replace multiplications by summations.

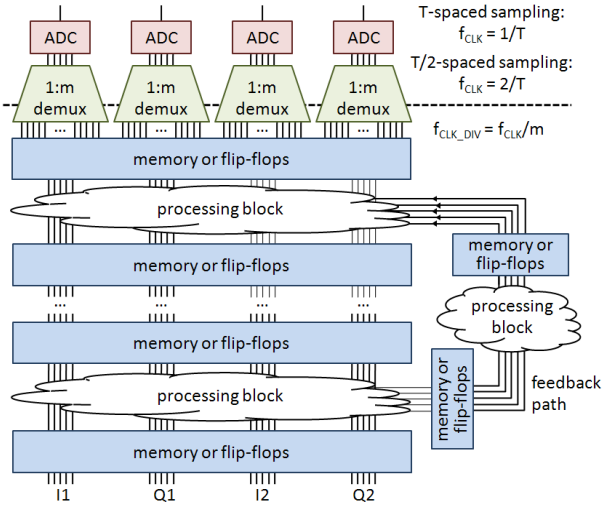

Fig. 2. Internal structure of the DSPU.

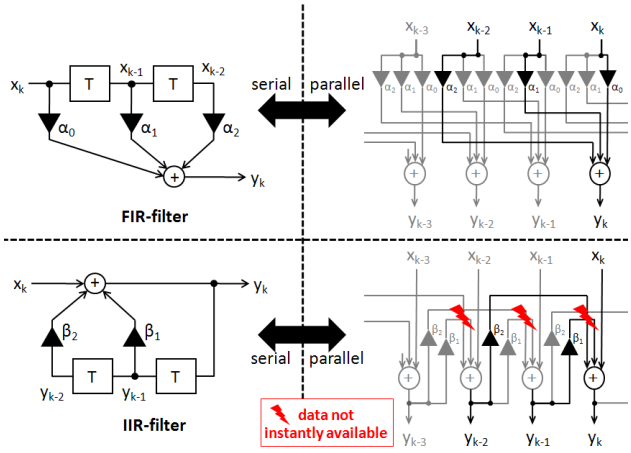

Fig. 3. Serial and parallel implementation of FIR- and IIR-filters.

The last important consideration if algorithms are suitable for real-time applications is the tolerable feedback delay. In simulation or offline processing feedback delays of 1 symbol are easy to achieve, but it is impossible in a real-time system. The reasons are the parallel processing and massive pipelining, which is required to cope with the high data rates. Pipelining means that only fractions of the whole algorithm are processed within one clock cycle and the intermediate results are stored in buffers (e.g. memory or flip-flops) as shown in Fig. 2. Therefore it can take easily >100 symbol durations (~10 ns @ 10 Gbaud), until a received symbol has an impact on the feedback signal. For polarization control or CD/PMD compensation, which in general use integral controllers with time constants in the µs-range [3], the several nanoseconds additional delay due to pipelining can be neglected. But the feedback delay can have a severe impact on the performance of algorithms that require an instantaneous feedback, e.g. decision-directed carrier recovery, which is often used in offline signal processing for higher order QAM [6].

3. Integrated circuits for a real-time coherent QPSK receiver

In the framework of the synQPSK-project funded by the European Commission the University of Paderborn has developed integrated circuits for a 40 Gb/s real-time coherent QPSK receiver.

A 5 bit 12.5 Gs/s analog-to-digital converter (ADC) was designed in a SiGe technology [8]. For the layout a pure flash topology without a track-and-hold amplifier was chosen to obtain the necessary input bandwidth and sampling speed. A pipelined EXOR logic transforms the resulting 31-bit thermometer code first into a 5-bit Gray-encoded signal, then into binary encoded output signals. The detour to Gray coding is advantageous because it gives a higher immunity to bubble errors in the initial thermometer code than direct binary encoding. The power consumption of the ADC is measured as ~2.7 W.

To perform polarization control and carrier & data recovery a CMOS circuit was designed. The chip first parallelizes the input data from the ADCs into 16 data streams. The 1:16 demultiplexer consists of a 1:8 demultiplexer in a full-custom design that can process input data rates up to 10 Gb/s, and a 8:16 demultiplexing stage in a standard cell design. The combination of full-custom and standard cell design is necessary because CMOS standard cells only tolerate clock frequencies up to 1.5 GHz in the utilized technology.

After demultiplexing into parallel modules, the four 5 bit input vectors multiply a complex matrix M to compensate for polarization crosstalk and polarization dependent loss (PDL). The matrix multiplication is followed by the carrier & data recovery that uses an angle-based approach. Working in the angle domain reduces the hardware-effort, because complex multiplications are replaced by summations. The polarization control matrix is updated in a decision-directed approach by correlating the data before and behind the decision circuit within one out of the 16 parallel modules. The polarization control time constant can be switched between $c_1 = 0.4$ µs and $c_2 = 1.6$ µs (@ 10 Gbaud) by changing the control gain between $g_1 = 2^{-8}$ and $g_2 = 2^{-10}$ through an asynchronous serial debug interface. Together with this interface also other test and debug structures like a built-in self-test or BER counters are included on the chip to ease testing and configuration. The chip has a total complexity of 1.23M transistors in the standard-cell part, 12k transistors in the full-custom part and a power consumption of ~2 W.

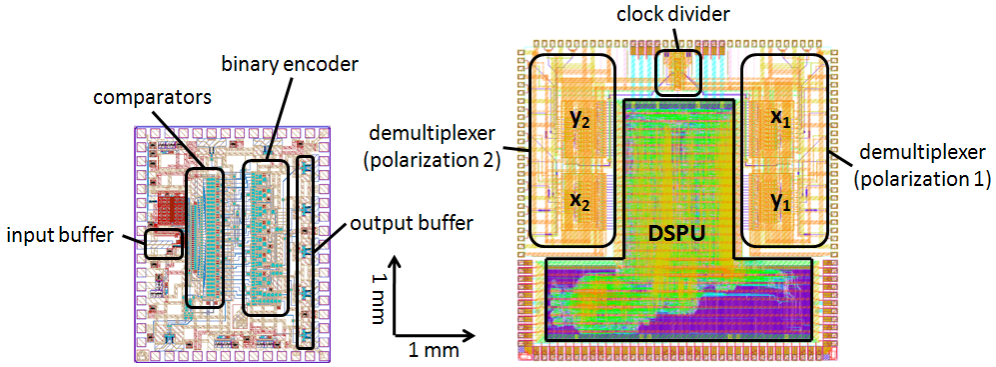

Fig. 4. Layout of a 5 bit 12.5 Gs/s ADC in SiGe technology (left) and a CMOS chip for demultiplexing, polarization control and carrier & data recovery (right) for a 40 Gb/s coherent polarization-multiplexed QPSK receiver.

4. Summary

We have derived three basic constraints for algorithm development for real-time digital coherent receivers: Feasibility of parallel processing, hardware efficiency and consideration of feedback delays. Additionally we have presented the layouts and design considerations of an ADC and a CMOS DSPU for a 40 Gb/s coherent polarization-multiplexed QPSK receiver.

5. References

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