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Multiplier-Free Realtime Phase Tracking in Digital Synchronous QPSK Receiver for Coherent Optical Detection

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Abstract- A multiplier-free phase estimation algorithm based on the barycentre approach for coherent QPSK detection is presented. A selectivity mechanism was developed that significantly improved its performance. In addition to recently published measurement results, theoretical background and new simulation results are presented.

I. INTRODUCTION

Quadrature phase shift keying (QPSK) is the modulation format most likely to be employed for the first generation of 100 Gbit/s transmission systems. Implementations of coherent detection with high-speed digital signal processing (DSP) usually employ feedforward phase estimator structures in their data recovery [1-3].

To obtain a modulation-free reference phase, the most common method is the Viterbi and Viterbi (V&V) phase estimator [4]. The disadvantage of this algorithm for which an optimization has been presented [5] is that it requires several coordinate conversions and complex calculations including multiplications in its lowpass filter. We present a multiplierfree phase estimator with high phase noise tolerance suitable for 10 GBaud systems with DFB lasers.

II. THEORY

The received symbols can be described as a sequence of complex numbers Z(k) that consist of the QPSK symbol multiplied by a time-variant phasor, and additive channel noise. The position angle of the received symbol within its quadrants is defined as

$$\mathcal{G}(k) = \left(\arg(Z(k)) \mod \frac{\pi}{2}\right). \tag{1}$$

The position angles $\mathcal{P}(k)$ do not depend on the sent QPSK symbols and thus a V&V phase estimator can employ them to generate unimodular complex numbers. For phase estimation, they are usually lowpass-filtered by a complex summation (average) over windows with 2N+1 values:

$$\hat{\phi}(k) = \frac{1}{4} \left[\arg \left(\sum_{n=k-N}^{k+N} \exp(4j \,\vartheta(n)) \right) \mod 2\pi \right]$$
(2)



Fig. 1. The improved basic cell generates an estimated average angle μ from the sum and the difference of two input angles as well as one-bit reliability information.

Alternatively, the set of modulation-free position angles $\vartheta(k-N), \vartheta(k-N+1), ..., \vartheta(k+N)$ can also be used to obtain an estimated phase $\hat{\varphi}(k)$ immediately, i. e. without function tables and complex calculations. The barycenter algorithm converts pairs of position angles α, β into a single average position angle μ by a non-complex basic cell (bc) function [6]. Such bc functions $\mu(\alpha, \beta)$ are concatenated to a phase estimation tree, and the partial result from each basic cell can be expressed in a complex description as

$$\mu = \frac{1}{4} \left(\arg \left(e^{j4\alpha} + e^{j4\beta} \right) \mod 2\pi \right). \tag{3}$$

The hardware for each bc are only two adders that generate the sum and the difference of the input angles in parallel and a simple Boolean unit that finally calculates μ without an additional processing cycle [7]. The bc delivers the average phase of two normalized phasors, but the magnitude information is not preserved for the subsequent cells. It has been proposed to extend the basic cell function by a coarse magnitude calculation and to use this information in subsequent bc formulas [8]. But this requires much more effort because the bc formulas are modified.

Fig. 1 shows the internal structure of an improved bc in the first processing stage. The magnitude information corresponding to μ does not have to be calculated. Instead, the already employed angle difference $\delta = \alpha - \beta$ allows determining whether the result is reliable. The reliability is almost equivalent to a high magnitude of the complex sum in (3), but it can be calculated with less effort and encoded into a single bit by the following assignment

$$R(\mu) \coloneqq \left\lceil \frac{1}{2} - t + \left| \delta \right| - \frac{\pi}{4} \right\rceil$$
(4)

where *t* is an appropriate threshold value and $\lceil x \rceil$ denotes the smallest integer that is greater than x.

A Boolean function in subsequent stages uses pairs of reliability bits to decide whether the regular bc formula should be used or a non-reliable input value should be dropped in favour of the better one. If input α is marked as reliable and β is not, the assignment $\mu := \alpha$ simply bypasses the bc formula. Instead of a formula modification, only a selector switch (multiplexer) is necessary for this selectivity mechanism [7]. The switch is set while the bc value is generated. Because of the selectivity mechanism, our algorithm is called Selective Maximum Likelihood Phase Approximation (SMLPA).

If a single reliable input value is selected to replace the bc output value, it also inherits its reliability property for the next stage. Otherwise, a new reliability bit is generated in parallel with the average value. Therefore, two non-reliable input values can produce an output value marked as reliable under the condition that they confirm each other.

III. SIMULATION RESULTS

We present a comparison of three different phase estimators that employ the same input information: N=4 mean that 2N+1=9 position angles are used to estimate the center value. For reference, an asynchronous receiver (no phase estimation) is also simulated. Transmission of 200 million symbols was simulated (Monte Carlo).

For Fig. 2, we assume a 10 GBaud system with DFB lasers which low phase noise requirements on the receiver (laser sum linewidth: 1 MHz) and an uncompensated laser frequency mismatch of 16 MHz. The V&V estimator performs best, but the curves of the barycenter estimator is very close to it. The improvement of SMLPA compared to barycenter is small but visible.

Fig. 3 shows results for the same system but a laser sum linewidth of 10 MHz which were to be expected for standard DFB lasers. Only the V&V phase estimator BER curve exhibits a floor characteristic. The barycenter and SMLPA algorithms are tolerant to this high linewidth, as well as the



Fig. 3. Simulated BER with high phase noise requirements (DFB lasers, sum linewidth = 10 MHz).

asynchronous receiver.

In Fig. 4 the obtained simulation results are verified experimentally [9]. Only a small implementation induced penalty is observed for the comparison of the measured to the simulated BER floors for the SMLPA. Both curves clearly outperform the V&V estimator, which exhibits an up to 1 decade higher BER floor.

IV. HARDWARE IMPLEMENTATION

The algorithm can be embedded to a FPGA [9-11] or to an ASIC [1, 2, 9, 12] along with other necessary algorithms (i.e.: clock recovery, polarization control & equalization, data recovery, and intermediate frequency control algorithms). First the inphase (I) and quadrature (Q) components of the received QPSK signal should be A/D converted [2, 13] using a high-speed A/D converter with a suitable resolution. The A/D converter output channels operate at a high data rate (e.g.: 10 Gbit/s). The CMOS logic based DSPU can not operate at such high data rates. Therefore, it is necessary to demultiplex [2] the A/D converter output data to a lower data rate (i.e.: 1.25 Gbit/s). The current FPGA technology could achieve up to about 2.5 GBaud data rate [10]. ASIC implementations are capable of operating at about 10 GBaud [1, 2, 12]. With the shrinking device sizes in the MOS technology it would be possible to achieve even higher data rates. Fig. 5 shows the block diagram of a coherent QPSK with polarization multiplex receiver.



Fig. 2. BER simulation with sum linewidth = 1 MHz.



Fig. 4. Simulated and measured BER floors for different carrier recovery algorithms.



Fig. 5. Block diagram of a coherent QPSK with polarization multiplex receiver.

V. CONCLUSIONS

We have presented an improved realtime phase tracking algorithm for a coherent QPSK receiver with low hardware effort and high phase noise tolerance. Employing the anglebased barycenter approach, complex calculations and coordinate conversions are avoided. A substantial improvement called selectivity mechanism is explained in detail. Earlier experiments validate the theory.

ACKNOWLEDGMENT

The authors like to thank the financial support received from the European Commission (EC) and the German Academic Exchange Service (DAAD).

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