5-bit 12.5 Gsamples/s Analog-to-Digital Converter for a Digital Receiver in a Synchronous Optical QPSK Transmission System

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Abstract — **We present the implementation of an analog-to-digital converter in a SiGe BiCMOS technology. The converter has a resolution of 5 bits with a sampling rate > 12.5 Gsamples/s and consumes 4.3 W of power.**

Index Terms — **Optical communication, analog-to-digital converter, quadrature phase shift keying, synchronous detection, real-time systems.**

I. INTRODUCTION

Coherent optical transmission combined with QPSK modulation allows a more efficient utilization of available bandwidth of existing optical fiber, together with the ability to mitigate all linear fiber distortions in the electronic domain. A critical component in a real-time optical QPSK receiver is the high-speed analog-to-digital converter (ADC) to digitize the incoming inphase and quadrature signals before subsequent digital signal processing (DSP). Several real-time implementations of a coherent transmission system were previously demonstrated at lower data rates [1,2], where the commercial ADCs and successive FPGA-based DSPs are the limiting factor. A coherent transmission system with a total data rate of 40 Gbit/s was presented with a full-custom DSP chip including high-speed ADCs [3]. Furthermore, several research publications presented ADCs at comparable sampling rates of $\geq$ 10 Gsamples/s, but none of them are commercially available [4,5]. This paper presents a 5-bit flash-ADC for sampling frequencies $f_{sampling}$ > 12.5 GHz and a full scale range voltage V_{FSR} = 500 mV in a bipolar SiGe technology.

II. CIRCUIT DESIGN AND IMPLEMENTATION

The 5-bit ADC was designed in a pure flash topology to obtain the necessary input bandwidth and sampling speed. Following the input buffer with the reference voltage generation are 2^5 - 1 comparator stages consisting of a pre-amplifier and two clocked latches to sample the incoming signal (see Fig. 1). A pipelined EXOR logic transforms the ensuing 31-bit thermometer code into a 5-bit Gray encoded output signal. The appropriate comparator outputs are combined using a binary tree structure with clocked EXOR-gates on each node [6]. Pipelined Gray encoding is more immune to bubble errors in the initial thermometer code than

common binary encoding, thereby eliminating the need for extra error correction circuitry.
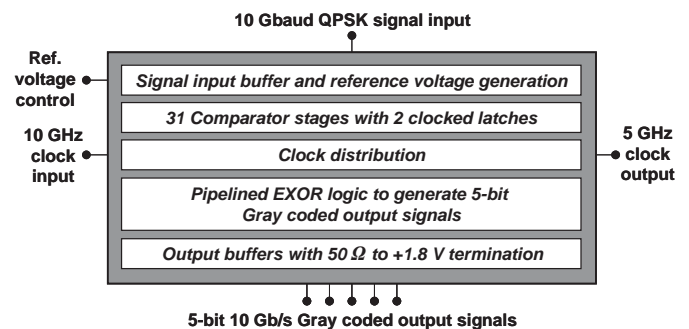

Fig. 1   Blockdiagram of the 5-bit flash-ADC.

Differential output buffers with 50 Ω termination to a +1.8 V supply are interfacing the digitized signals to a successive CMOS DSP circuit for carrier recovery and further processing. A half rate (5 GHz) clock output is also implemented to synchronize the DSP circuit.

The ADC was manufactured in a 0.25μm SiGe:C BiCMOS technology with a transit frequency f_T = 120 GHz, a maximum oscillation frequency f_{max} = 140 GHz, and an emitter-collector breakdown voltage V_{CEo} = 2.3 V [7]. Fig. 2 shows a photograph of the designed ADC chip.
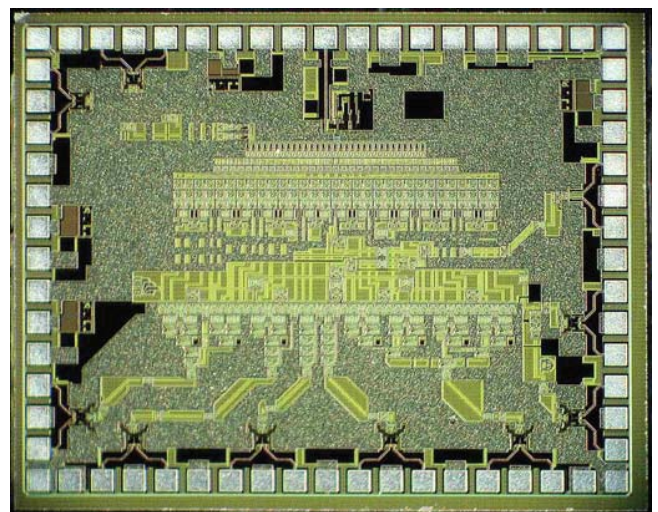

Fig. 2   Photograph of the 5-bit ADC chip.

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Due to the necessary number of pads the overall chip is pad-limited in size and measures 2.25 mm x 2.85 mm. A total count of 5078 active and passive devices including 3296 transistors are integrated in the ADC circuit. The sum power consumption of the ADC is 4.3 W, with –4 V and +1.8 V supply voltages.

A suitable mounting fixture was designed to facilitate appropriate testing of the ADC. It consists of an Al_2O_3 ceramic substrate with 50 Ω coplanar signal lines, soldered 1.2 mm semi-rigid coaxial cables and a copper heat sink.

III. MEASUREMENT RESULTS

Fig. 3 shows the measurement of the differential and integral non-linearities (DNL/INL) conducted with a sampling frequency of 10 GHz. A low speed ramp signal at the input covered the full scale range voltage V_{FSR} = 500 mV with no missing output codes. Both the DNL and INL stayed within ±0.25 LSB (least significant bit), therefore displaying excellent linear behavior over the full input range, even with the fast sampling clock applied.
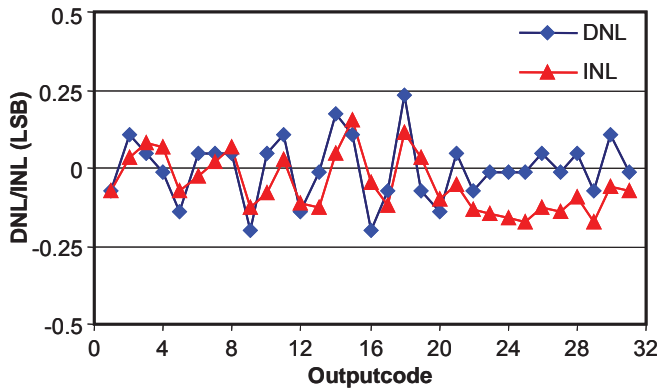

Fig. 3   Measured differential and integral non-linearity (DNL/INL) with $f_{sampling}$ = 10 GHz.

To measure the dynamic characteristics of the ADC a sinusoidal input signal was applied with a frequency f_{in} = (31/64) * $f_{sampling}$. This forces the Gray encoded output signals to repeat every 64 bits, while still using the highest possible Nyquist frequency at the input.

Fig. 4 shows the measured Gray encoded output data bits D0 (LSB) to D4 (MSB) for sampling rates of 5 and 12.5 Gsamples/s with the corresponding input signals f_{in} = 2.42 GHz and 6.055 GHz. The input signal amplitude was set to V_{FSR} = 500 mV$_{pp}$. It can be seen that the output data repeats every 64 bits (vertical bars in Fig. 4) and tracks the expected output codes at both sampling rates (verified in simulation). The remaining small variations in the symmetry are caused by a slight frequency mismatch of the utilized signal sources.

Unfortunately, it was not yet possible to measure the effective number of bits (ENOB) directly, due to an unavailability of a suitable digital-to-analog converter. But in simulation the ADC achieved an ENOB = 4.5 up to $f_{sampling}$ = 15 GHz with a full Nyquist input signal.

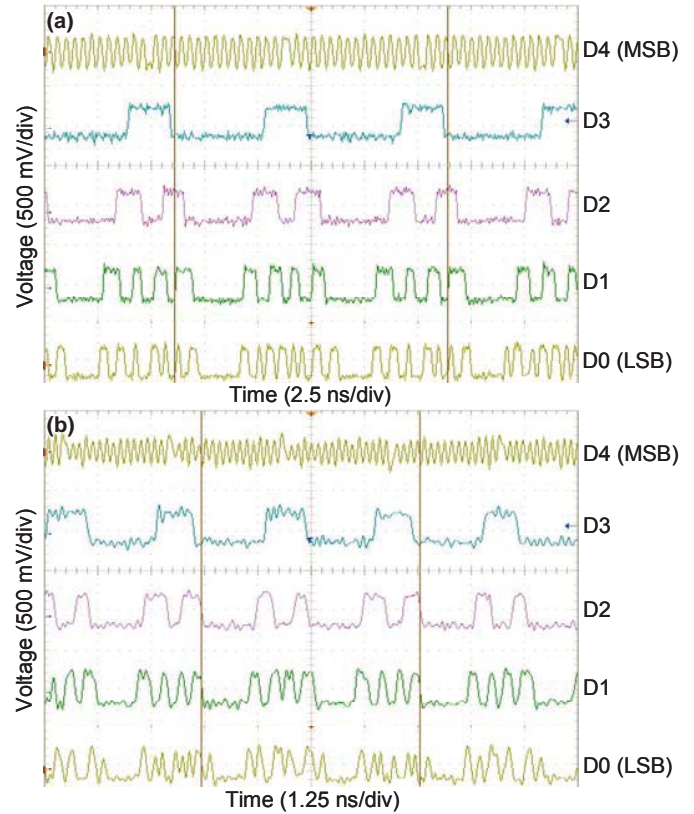*Fig. 4   Measured Gray encoded output data bits with (a) $f_{sampling}$ = 5 GHz and f_{in} = 2.42 GHz and (b) $f_{sampling}$ = 12.5 GHz and f_{in} = 6.055 GHz (input amplitude 500 mV$_{pp}$).*

IV. CONCLUSION

We have designed and mounted a 5-bit flash-ADC as part of a digital receiver in a coherent optical transmission system. The ADC exhibits exceptional linear behavior and supports sampling rates beyond 12.5 GHz. The chip measures 6.4 mm^2 and consumes 4.3 W of power.

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