Boosting Dynamics of AC Machines by using FPGA-Based Controls

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Abstract

The main focus of the following contribution is to point out the advantages of Field Programmable Gate Arrays (FPGAs) as a realization platform for AC machine controls in comparison to state-of-the-art Digital Signal Processor (DSP) based controls. Initially some important details of DSP based controls and the calculation of the achievable control bandwidth as a function of the chosen design parameters (e.g. sampling rate and strategy) are presented. It will be pointed out which constraints of DSP based realization lead to a limited control bandwidth. On the basis of the extracted results the FPGA-based quasi-continuous control is introduced and it is shown how the control bandwidth can be increased even if the switching frequency of the pulse width modulation (PWM) module is kept constant.

1. Processor-Based AC Machine Control

1.1. Torque and Current Control

Starting point for the following studies is the very well known cascaded control structure, which was first introduced for AC machines in the early 1970s together with the Field-Oriented Control (FOC) approach. The structure consists of an inner current or torque control loop with outer speed and position control loops as shown in Fig. 1. The following discussion will be restricted to the inner current control loop.

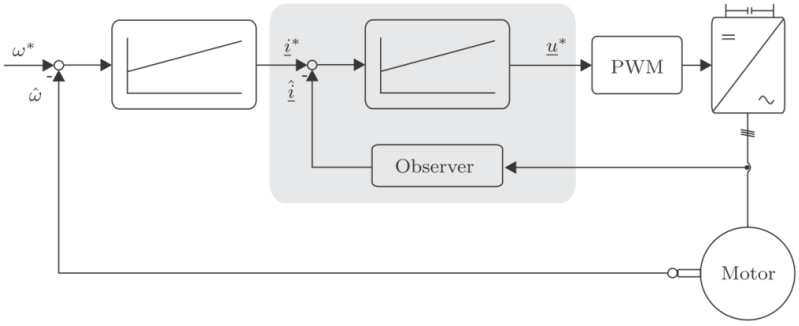


Fig. 1. Cascaded Control Structure for AC machines

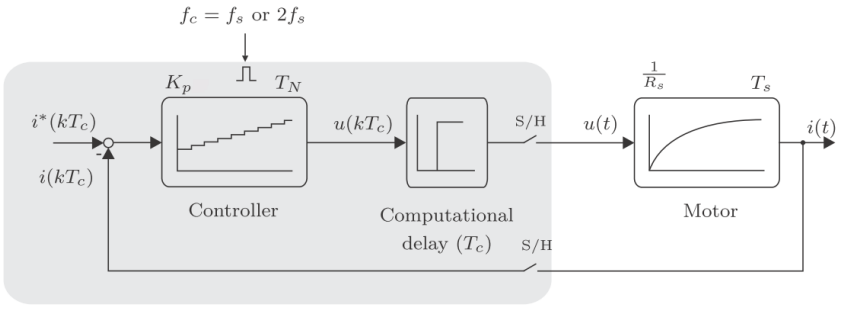
Traditionally Digital Signal Processors (DSPs) or microcontrollers (µCs) are used to realize the inner current control loop. State of the art for the digital control realization is the regular sampling approach which is introduced in the section 1.3. The basic idea is to synchronize the PWM, the data acquisition and the controller sampling to acquire only the fundamental sinusoidal signal of the motor current.

1.2. Achievable Current Control Bandwidth

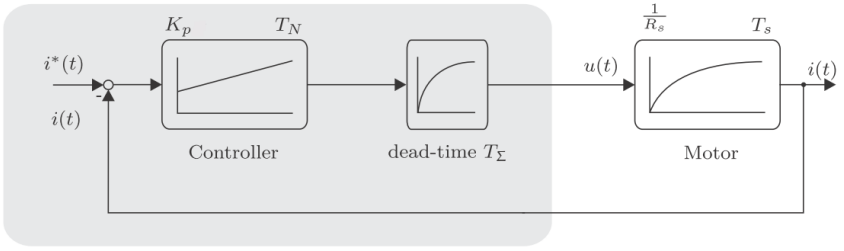
From standard control engineering textbooks [6] it is very well known, that the overall control system dynamics, which can be achieved with the mentioned cascaded control structure are limited by the inner control loop bandwidth. Therefore it is important to achieve the highest current control bandwidth possible. In order to calculate the achievable closed-loop control bandwidth, first a corresponding model has to be derived, that represents the dynamical plant behavior with sufficient accuracy. In case of regular sampling the PWM module can be considered as a simple unity gain (Fig. 2) (unlike the sample/hold an computational delay the PWM itself does not introduce any phase shift or delay). Due to the mentioned synchronization, the controller only acts on the current fundamental and the current ripple produced by the PWM voltage is not acquired. Therefore, the controller output reference voltage signal is only the fundamental sinusoidal signal, as well.

Introducing the quasi-continuous control in the next chapter the PWM module is allowed to accept continuously varying reference signals. Hence, the impact of the PWM Module has to be considered more carefully.

Within the closed control loop all different delay times sources are summed up in a total dead time T_Σ, that is mostly considerably smaller than stator time constant $T_\Sigma < T_s = L_s/R_s$. To consider the impact of the total time delay within the model there are two alternative approaches which are illustrated in Fig. 2.



(a) Equivalent model for control design



(b) Approximated model for control design

Fig. 2. Equivalent and approximated model for control design

However, measurement-based model validations in [3] have shown, that the approximation of the actual plant using a dead time (Fig. 2 a)) is more realistic than the PT2 approximation (Fig. 2 b)). Therefore, the following considerations are based on the dead time approach. If the commonly preferred PI-Compensator are used as current controllers, the open-loop transfer function $L(s)$ results to

$$L(s) = K_p\left(1 + \frac{1}{sT_N}\right)e^{-sT_\Sigma}\frac{1}{(R_s+sL_s)} \tag{1}$$

Assuming that the stator time constant $T_s = L_s/R_s$ is the dominant time constant $T_\Sigma < T_s$ in the open-loop transfer function $L(s)$ the controller parameter can be designed with analog

design rules e.g. Magnitude Optimum [6]. The controller reset time is set to $T_N = T_S$ in order to cancel the plant pole and the gain K_p is selected such that the closed-loop response has the damping $\xi = 1/\sqrt{2}$ resulting in $K_p = (R_s T_N)/(2T_\Sigma)$. Controllers designed with the Magnitude Optimum are known to have a good reference response, but however, a bad disturbance response. Assuming, that in most applications the disturbance reaction is not crucial the design with Magnitude Optimum is justified. The achievable bandwidth can be roughly estimated from the first-order approximation of the closed-loop transfer function from Fig. 2 b):

$$T(s) = \frac{1}{s^2 2T_\Sigma^2 + s2T_\Sigma + 1} \approx \frac{1}{s2T_\Sigma + 1} \tag{3}$$

Hence the approximated closed-loop bandwidth can be estimated with $BW \approx 1/(2T_\Sigma)$. Even if it is just a rough estimate it can be seen, that the limiting factor is the total dead time T_Σ within the closed loop. Consequently T_Σ should be reduced as much as possible to achieve a high bandwidth.
To show the increase of the achievable bandwidth in the second chapter (introducing FPGAs as realization platform), the switching frequency is fixed to $f_S = 5\,\mathrm{kHz}$ for the following studies. Hence, the controller sampling frequency of $10\,\mathrm{kHz}$ can be derived in case of regular sampling (Fig. 4 b)) and the total dead time results to $T_\Sigma = 150\,\mu\mathrm{s}$. The theoretical achievable bandwidth $BW_{th} \approx 1.2\,\mathrm{kHz}$ $(7.5\,\mathrm{ks}^{-1})$ for this configuration can be derived from the closed-loop bode plot using the dead-time approximation shown in Fig. 3.

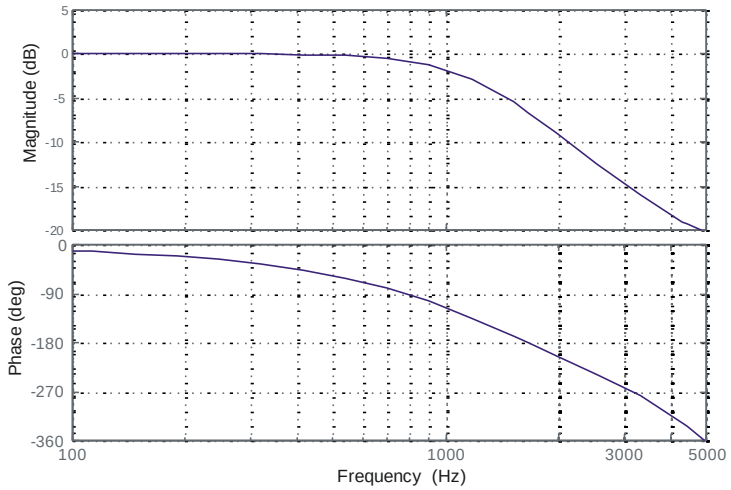


Fig. 3. Bode plot of closed-loop transfer function

The presented example demonstrate that, even with a high sampling frequency of $f_S = 5\,\mathrm{kHz}$ the achievable bandwidth is only few $100\,\mathrm{Hz}$ which may be adequate for standard drives, but is not sufficient for high performing servo drives. The limited bandwidth leads to low dynamic reference signal tracking, low disturbance rejection for higher frequencies and especially to poor suppression of torque/ current harmonics due to non sinusoidal back EMF. This limitation may even reduce the utilization of the motor and inverter, because good utilization is mostly ensured with sinusoidal currents. In practice the maximal bandwidth is limited by the switching inverter frequency f_s, therefore, to achieve the best possible performance the objective should be to increase the bandwidth close to the switching frequency. In the following different sampling strategies, along with the resulting total dead times are described for a predefined switching frequency.

1.3. Sampling Strategy

As mentioned before, all small time constants occurring in the closed current control loop are summed up in the total dead time T_Σ. However, the main portion is caused by the computational delay and measurement sampling. With the control sampling time T_C an effective dead time of $T_\Sigma \approx 1.5\,T_C$ can be assumed by applying the regular sampling approach ($1T_C$ is caused by the computational delay of the control algorithm and an additional delay of $0.5T_C$ can be ascribed to the sample and hold mechanism) cf. Fig. 3 a, b. With typical switching frequencies of standard industrial drives in the range of $5-10\,\mathrm{kHz}$ the controller sampling frequency can be assumed to $5-20\,\mathrm{kHz}$ if oversampling can be applied (provided the used µC has enough computational power to execute the control algorithm within the predefined computational time $T_C = T_S/2$).
Implementing the controller on a fast parallel processing FPGA instead of a sequentially working processor (case c) the computational delay of $1T_C$ can be neglected in the closed-loop reference-to-output transfer function and the total dead time reduces to $T_\Sigma \approx 0.5\,T_C$.
The effective total dead time can be reduced even more if oversampling rates higher than $OSR = 2$ are implemented using a FPGA and allowing the PWM Module to accept continuously varying reference voltage signals (case d). In this case not only the computational delay but also the total dead time is negligible and it is possible to achieve quasi-continuous control behavior.

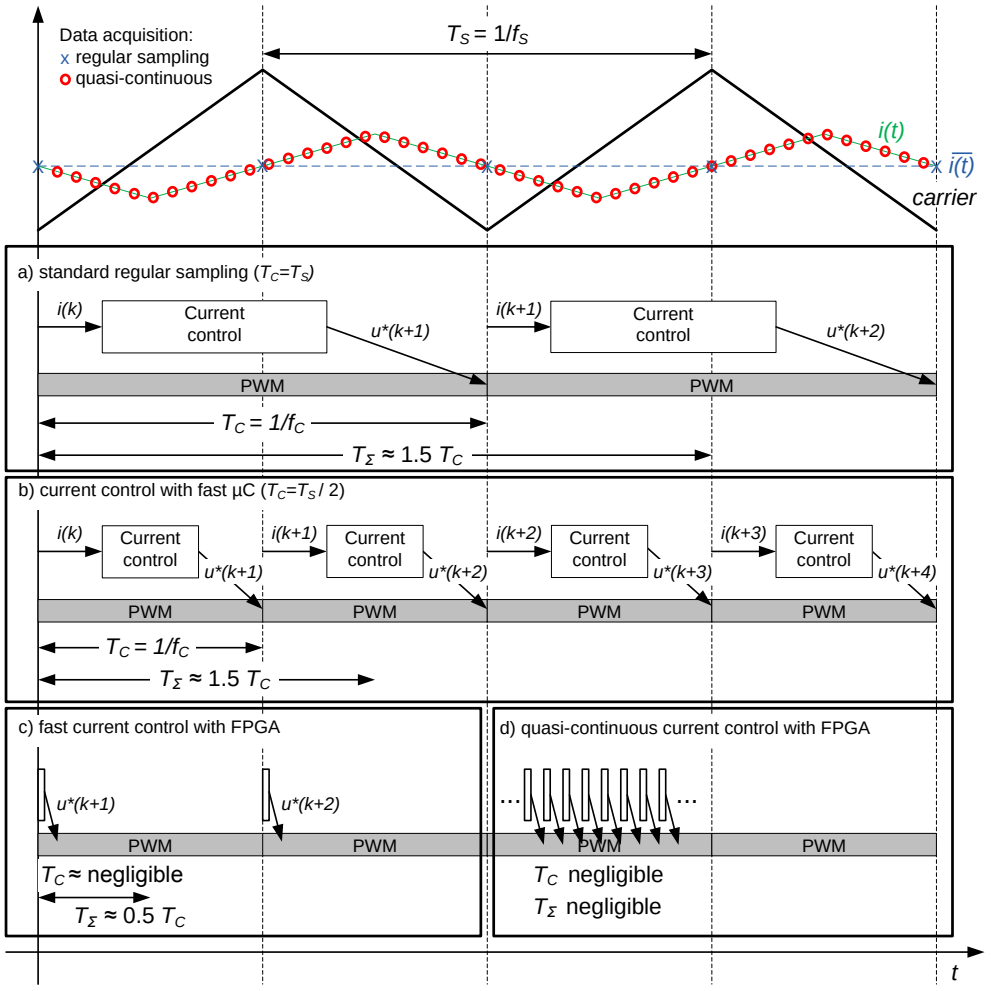


Fig. 4. Control processing task timing with different approaches

2. FPGA-Based AC Machine Control

2.1. Advantages of the FPGA

With the presented regular sampling control approach the achievable bandwidth is considerably restricted due to the inevitable high total dead time. To achieve the best performance of the whole control system it is crucial to reduce the dead time. Therefore, FPGAs are getting more and more in the focus as realization platform for high performance servo drive applications.

The drops in pricing throughout the recent years as well as the progress in the provided tools to develop applications and program the FPGAs has made them more and more popular in drive control applications. The inherent feature of FPGAs lies in its parallel execution capabilities together with high sampling rates in the range of MHz.

To justify the use of FPGAs to enhance the dynamic capabilities compared to processor-based applications, without increasing the switching frequency, not only the enhancement in achievable bandwidth but also the occurring total harmonic distortion (THD) of the motor line currents should be evaluated.

2.2. Quasi-Continuous Current Control

Minimizing the computational time (around a few hundred ns) and allowing the PWM module to accept continuously varying reference signals it is possible to achieve quasi continuous behavior on a digital platform. Therefore, the PT1 element which represents the dead time in Fig. 2 (b) can be neglected for further studies and the dynamical behavior of the plant reduces to a simple PT1 element. Hence the achievable bandwidth becomes very high (limited by the switching frequency). The resulting control structure is shown in Fig. 5.

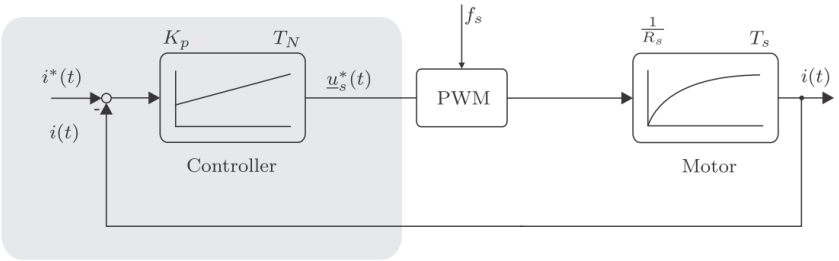


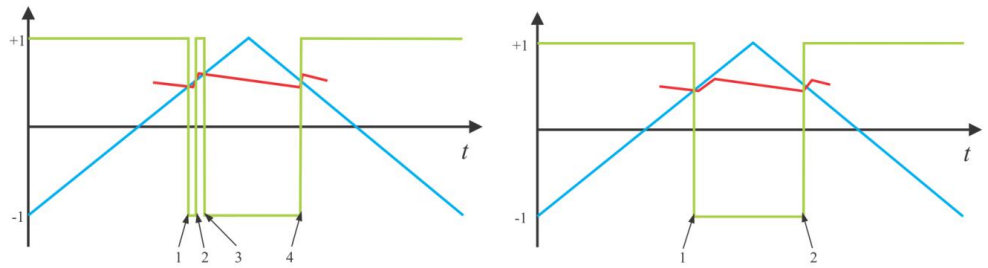
Fig. 5. Quasi continuous control

If continuously varying voltage reference signals are supposed to be applied to the PWM, only carrier-based PWM is feasible while Space Vector Modulation is not. Furthermore, the PWM module has to be designed carefully, because in contrast to the regular sampling approach the controller not only acts on the fundamental sinusoidal current, but also on the ripple produced by the PWM voltage. Hence, there is no filtering of the switching frequency components in the feedback current signals and the controller gain has to be adapted to the new circumstances [4].

Considering the mentioned points leads to following basic design criteria:

- no more than two switchings in one PWM period are allowed
- the voltage reference signal should never be forced into saturation region in steady-state operation, even for a short time

To ensure that no more than two switchings per PWM period appear the slope of the reference voltage signal has to be limited. If the slope is equal or higher compared to that of the modulation carrier (Fig 6 (a)) the basic condition is violated, otherwise if it is lower (Fig. 6 (b)) it is ensured that the basic condition is kept.



(a) Reference-voltage slope higher than carrier (b) Reference-voltage slope lower than carrier

Fig. 6. Comparison between the reference voltage slope and the carrier slope

In highly dynamic applications the PI-controller can be approximated as high gain P-controller. The task of the integrator is only to compensate steady-state errors. Hence the reference voltage slope mainly depends on the control error signal. Due to the slow input reference current change compared to that of the measured current, the control error signal slope can be approximated as the slope of the d- and q- axis control error components. Therefore, the voltage equations can be evaluated for this requirement. Consequently, the slope of these currents depends on the motor speed (considered by the modulation index $M = \hat{u}^*/(V_{dc}/2)$) and load conditions (considered by the torque generating component i_{sq}). Evaluating the maximal allowable slope of the carrier in dependence of the switching frequency and the DC-link voltage the allowable maximum value in order to satisfy the first criteria can be derived to:

$$K_{pd} = \frac{2V_{dc}f_s}{max\left(\frac{di_{sd}}{dt}\right)}\ ; \qquad K_{pq} = \frac{2V_{dc}f_s}{max\left(\frac{di_{sq}}{dt}\right)} \tag{3}$$

Using these gains it is ensured, that no more than two switchings in one PWM period occur in each inverter leg. The derived maximum gains for the d- and q- axis now also have got to be adapted to the second constraint. The maximal voltage of an inverter is typically little bigger than the rated voltage of the motor, however, this margin voltage is only valid for the fundamental reference voltage component. Therefore, a reference-voltage signal superimposed by a switching ripple (in case of the quasi-continuous approach) obviously saturates the reference voltages in operation close to the rated motor speed. Hence, at lower speed this constraint is not crucial, while at higher speeds there is a very little margin resulting in relatively small gains. In the considered case the inverter has a voltage margin of 27% ($M = 0.73$ at rated steady operation of the specimen motor). To investigate the gain limitation due to the available inverter margin the occurring ripple current should be derived as a function of speed/ modulation index. Following the computational results for the controller gains considering both constraints are presented in Fig. 7 for a permanent magnet synchron motor (PMSM). The q- axis current is represented as normalized value $i_{sqN} = i_{sq}/I_N$ with respective to the rated quantity and the whole interval [0;1] is captured.

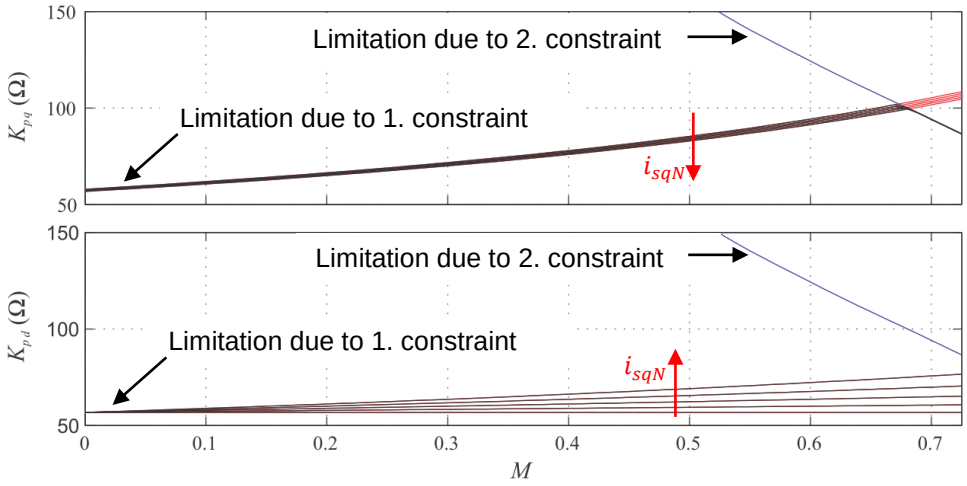


Fig. 7. Final gain selection as a function of modulation index M and load

It is obvious, that to satisfy both constraints the smallest gain values, represented by the black line, have to be chosen for respective operating points. Due to the variable gains the calculated closed-loop bandwidth is also varying as shown in Fig. 9 (the DC bus voltage is assumed to be constant in the whole operation range and the load applied is represented by $i_{sqN} = 1$). As expected the achievable bandwidth at the same switching frequency is higher compared to the bandwidth of $1.2\ \mathrm{kHz}$ of the processor-based approach.

In order to compare the dynamic performance of quasi-continuous and regular sampled controllers the THD of the motor currents should also be evaluated. Therefore, for regular-sampled controllers the purely sinusoidal reference signal (with “zero-sequence”) is used for calculation and for quasi-continuous controllers additionally the calculated ripple current multiplied with the controller gain is considered. The calculated THD for both approaches is presented in Fig. 8. It is obvious, that the difference is not at all considerable and it is possible to draw a conclusion, that the PWM attenuates switching harmonic reference components to a great level. Accordingly the approximation of the PWM behavior as a constant gain in the described quasi-continuous control design is justified for steady-state operation, hence, the PWM module in Fig. 5 can be neglected in steady-state case.

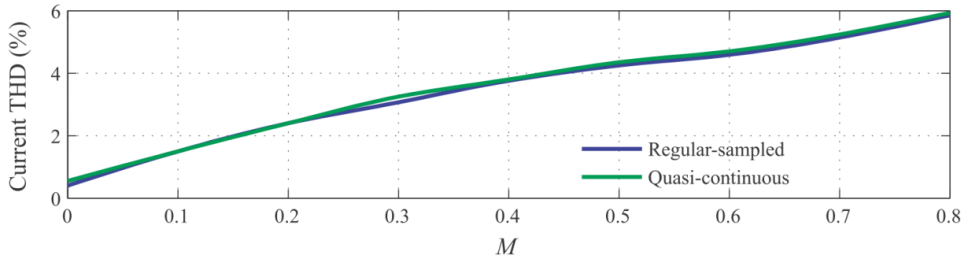


Fig. 8. Evaluated THD for both controller approaches

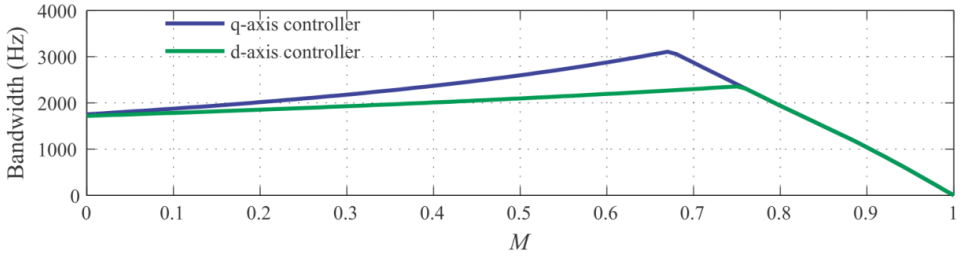


Fig. 9. Achievable closed-loop bandwidth with quasi-continuous controller

3. Summary

The comparison between state-of-the-art processor-based control realization and the quasi-continuous FPGA-based control realization has shown that the quasi-continuous approach has a very impressive dynamic performance. Consequently better reference tracking and disturbance suppression can be achieved. The enhancement is achieved without increasing the inverter switching frequency by utilizing the inherent FPGA features. The new approach is even with regard to the produced total harmonic distortion (THD) by the highly dynamic quasi-continuous controller always around the best possible range of regular-sampled control.

4. Literature

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