High Fidelity Hybrid Hardware-in-the-Loop Simulator with FPGA and Processor for AC Railway Traction

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Abstract

In this paper, a high fidelity hybrid real time hardware-in-the-loop (HiL) simulator using FPGA and real time processor is introduced and its application on an AC railway vehicle traction system composed of power electronic converter and induction motor is reported. By a novel computation load balancing, a reduced FPGA resource consumption and reduced delay introduced by HiL can be achieved. The closed-loop experiment with a three-phase induction motor controller shows that the proposed hybrid solution obtained almost the same computing precision as that of a pure FPGA HiL simulator.

1. Introduction

With the ever-growing intelligence and complexity of power electronic and drive system controllers, the real time Hardware-in-the-Loop (HiL) simulation has gradually established itself as an indispensible development and validation method in the past decade. In many high power applications like electric traction, the HiL simulation is becoming an indispensible facility in high coverage and reproducible tests of controller functions, like stress test and regression test of the traction control unit (TCU) of high power AC railway traction system [1] [2].

In a HiL simulation, the developed controller is the device under test and connected to a virtual plant in the identical way as it is connected to the real plant, such as inverter and electric machine. The virtual plant or the HiL simulator is composed of a real time computation machine (mostly a processor) calculating the mathematical model of the plant and specific I/O hardware emulating the sensor and actuator as is shown in Fig. 1

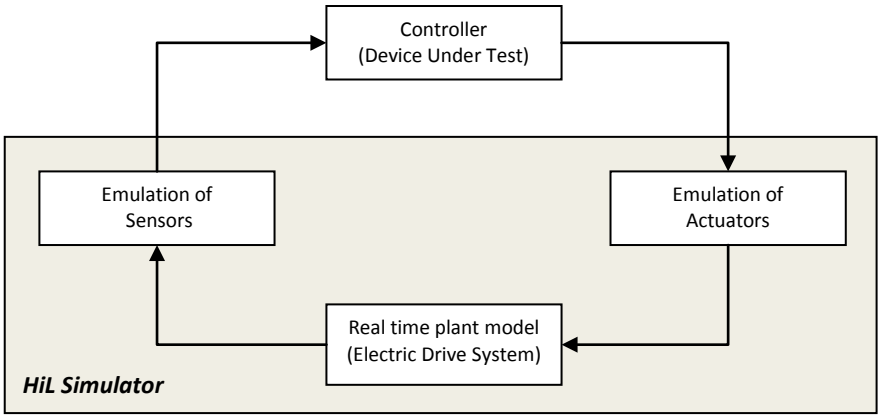

Fig.1. Hardware-in-the-loop simulation of controller

Since the HiL simulator works in real time and emulates exactly the electrical behavior of the actual sensor and actuator, the controller development could be directly carried out on the HiL simulator without waiting for the availability of the drive component prototypes or the risk of damaging them.

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2. State of the Art of HiL Simulator

The processor-based HiL simulator runs to its limit when it comes to modern electric drive systems that usually contain high speed power electronic switches. Modern traction electric drive controllers modulate the actuating variables (AC voltage with variable frequency and amplitude) into high speed switching signals to turn on or off the power electronic devices such as IGBTs. Unlike offline simulator, the HiL simulator works in real time and therefore employs deterministic fixed-step numerical algorithms. As a result, the HiL simulator runs asynchronously with the controller and makes a problem called inter-simulation time step switching (ITS) unavoidable [3]. Due to system software (real time operating system) and hardware (processor-I/O communication) overhead, the processor-based HiL simulator only samples the controller switching signals at a fixed time grid with relatively large time distance compared to switching period of the gating signals. The missed controller switching signals can lead to erroneous calculation of the drive system state variables and in worst case cause instability.

The state of art processor based HiL simulators for electric drive controller capture the switching events (so-called time stamping) that happen within one simulation time step by using special timing hardware and employ different compensation algorithms to account for these switching events [4]. Most of these compensation algorithms involve linear interpolation of the state variables on the instant of the missed switching event (the so-called time stamp) and linear extrapolation for one time step with another interpolation bringing the state variables back to the current time grid, a very good survey of widely used compensation algorithms can be found in [5].

Although the system state variables at the fixed time grid are accurately calculated, the downward limit on simulation step size due to sequential instruction execution and system software and I/O hardware overhead of the real time processor will cause a latency or so-called HiL delay that is usually much larger than the latency of the real plant, as is illustrated in Fig. 2. Since the missed switching events can only be accounted for at the next sampling time, the worst case delay could be larger than one simulation time step considering the hardware and software overhead. The commercially available real time processor can achieve a minimum time step around 20 µs running single AC machine and inverter model [6]. The real latency of power electronic inverters used in traction systems is usually much smaller. This additional delay will cause considerable discrepancies of a closed-loop HiL simulation compared with the realistic behavior of a real inverter and AC machine as reported in [1] and [7].

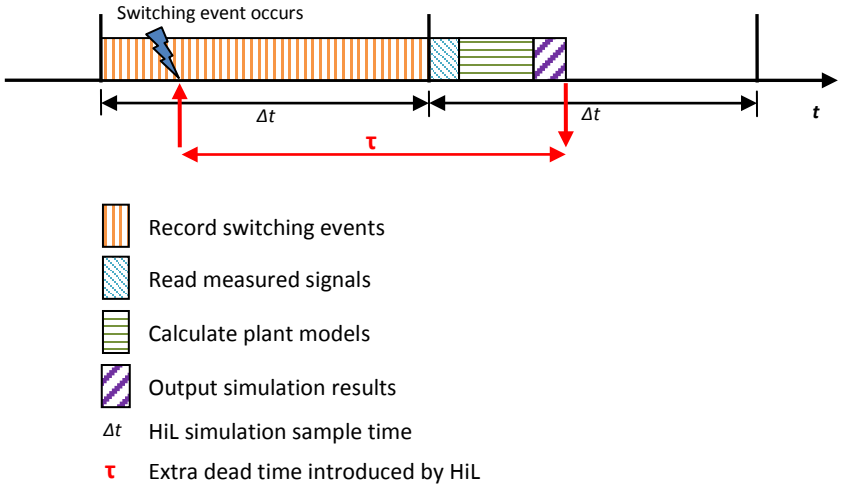

Fig.2. Extra dead time introduced by HiL simulator

The satisfactory solution to this problem would require extremely small simulation step size (several hundred nanoseconds), which is considerably smaller than the intrinsic overhead of processor based HiLs. To meet this challenge, the application of FPGA technology has been given lots of impulses in the past five years and thanks to its large scale parallel computing

architecture, the simulation time step has been reduced to several hundred nanoseconds for running models of power electronic converters and electric machines [3], [7].

Despite of all the advantages gained, the FPGA based simulator suffers from limited device resources (esp. when multiplier and divider are concerned) and longer compilation and synthesizing time of HDL design which compromises the flexibility of automatic controller tests usually exhibited by processor based HiL simulators. For railway traction applications, these limits are problematic due to following two facts

- Unlike in the electric or hybrid automotives, the drive train of railway vehicle contains more than one traction motor and power converter, for example, the 7200 kW electric locomotive developed by Zhuzhou Electric Locomotive Company has a C'o-C'o drive train which contains six induction machines and six power inverters. It is desirable to run the models of as many machines and inverters as possible.
- To diversify the product line, different drive train concepts are to be explored and studied, which puts a high requirement on model variants handling and parameter sets management, the long synthesizing time of the FPGA design makes the recompilation with different parameter set impractical and the communication bandwidth between FPGA and processor put a limit on the number and size of parameters that can be transmitted between processor and FPGA model.

In regard of these drawbacks of the otherwise very precise FPGA simulation, it is obvious that a more efficient computation load balancing between FPGA and processor could provide a possibility to utilize the potential of processor and FPGA in a more suitable way for HiL simulation of traction controllers.

3. Real-Time Simulation Model of Railway Traction System

For the drive train of modern railway vehicles, adjustable speed AC drives with three-phase rotating field motors and power electronic converters are becoming the de-facto industry standard due to their smaller size and easier maintenance compared with traditional DC drives. Based on different railway power supply infrastructure, two major types of AC drive topologies are employed today: in the first type, DC power supply is fed to voltage source inverters (VSI) and electric motors, as is usually applied in urban rail systems like metros or trams; in the second type, high voltage single phase AC power supply is fed through traction transformer first to active front end four quadrant converters (line side) and then the rectified DC voltage is fed to the VSIs and electric motors (motor side), as is commonly deployed in mainline locomotives and high speed trains [9].

In this paper we restrict our attention on the VSI motor topology shown in Fig. 3, since they are the most common and vital components in the drive train of almost all AC railway vehicles. In the circuit of Fig. 3, a two-point B6 topology with IGBTs is used for the VSI and a three-phase squirrel cage induction machine is used for traction motor.

For the real time HiL simulation, detailed transient models of power electronic device, as in offline simulation package like PSpice, can hardly be exploited because they are intrinsically computationally demanding and as such not suitable for fixed-point numerical solvers [3]. For testing the traction unit controller, the transient effects of power electronic devices are usually not the focus. For this reason and to achieve best simulation time performance, the power electronic devices are treated like ideal switches. The switching function approach as is described in [8] is used in real time modeling of the drive train traction circuit. The switching function of one single bridge is defined as a binary-valued function of gate switching signals $\boldsymbol{g}$ and circuit state variables $\boldsymbol{x}$. The dead time to avoid the bridge short circuit can be easily implemented since the switching function does not depend solely on the gate switching signals.

$$s = s(\boldsymbol{g}, \boldsymbol{x}) \in \{-1,1\} \tag{1}$$

In equation (1), $\boldsymbol{g}$ is the vector of switching signals from the controller; $\boldsymbol{x}$ is the vector of circuit state variables.

For the VSI, the equivalent switching function model considering the equation (1) is given in the Fig 3.

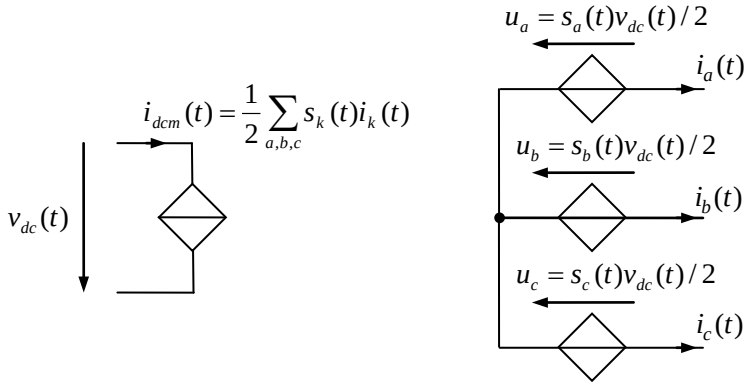

Fig.3. Equivalent circuit of VSI using switching function

Since the requirement of the HiL simulator is to reconstruct the real machine and inverter with minimum computation load, it is reasonable to base the state space equation on the stator coordinates and select the stator currents and rotor fluxes as state variables so that the controller feedback values (DC link voltage, stator phase currents and mechanical speed) can be directly derived from the state variables. Fig. 4 gives the dynamic two-axis stator coordinate-based induction machine model that is used in the HiL simulation, R_s, R_r denote the stator and rotor winding resistances, respectively, $L_{\sigma s}$, $L_{\sigma r}$ denote the leakage inductance of the stator and rotor windings, respectively, L_m denotes the mutual inductance between the stator and rotor windings, ω_{rs} is the electrical angular speed of the rotor.

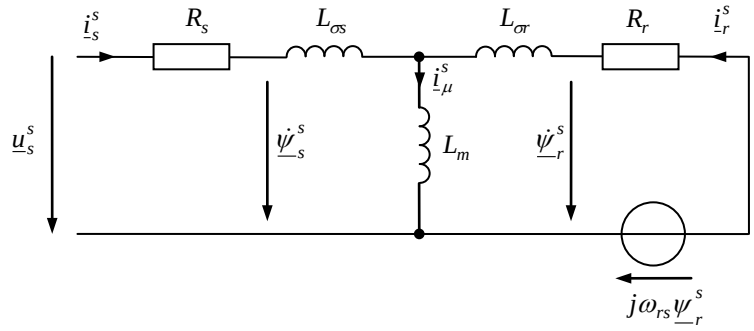

Fig.4. T-type equivalent circuit diagram of squirrel cage induction machine on stator coordinate

Assuming constant inductances and considering the slow changing rotor angular speed as a parameter, a continuous state space equation derived from Fig. 4 can be written in the form, where the elements of system matrix *A* and input matrix *B* can be found in [13]

$$\begin{bmatrix} \dot{i}_{s\alpha} \\ \dot{i}_{s\beta} \\ \dot{\psi}_{r\alpha} \\ \dot{\psi}_{r\beta} \end{bmatrix} = A(\omega_{rs}) \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \\ \psi_{r\alpha} \\ \psi_{r\beta} \end{bmatrix} + B \begin{bmatrix} u_{s\alpha} \\ u_{s\beta} \end{bmatrix} \tag{2}$$

In Equation (2) the system input vector $\left[u_{s\alpha}\ u_{s\beta}\right]^T$ is yielded from the Clark transformation of the output voltages of VSI as shown in Fig 3, written in matrix form

$$\begin{bmatrix} u_{s\alpha} \\ u_{s\beta} \end{bmatrix} = C \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = C \begin{bmatrix} s_a(t)v_{dc}/2 \\ s_b(t)v_{dc}/2 \\ s_c(t)v_{dc}/2 \end{bmatrix} \tag{3}$$

Here *C* is the Clark transformation matrix.

To implement the dynamic model on the HiL simulator, Equation (2) must be converted into discrete-time model by selecting a proper numerical solver and simulation step size. The selection of numerical solver and simulation step normally has a significant impact on the performance of HiL simulator. The guidance of selection involves three factors:

- To guarantee the numerical stability with certain margin
- To keep the numerical error as small as possible
- To achieve minimal computation load for real time requirement

Among frequently used fixed-step solvers, the explicit Euler solver takes the minimal computation load and thus has the best time performance. However, the explicit Euler has the drawback of small stability region; therefore the simulation step must guarantee the numerical stability. Since the system matrix *A* contains the variable parameter of electrical rotor angular speed, the loci of its eigenvalues with rotor angular speed as parameter on the complex plane must be employed in the investigation of numerical stability. Both theoretical analysis [11] and practical experience [13] show that for a wide speed range (0 to 5000 min^{-1}) and typical large machine rotor time constant (< 100 ms), a time step smaller than 50 µs suffices to ensure forward Euler stability criterion with a large margin.

4. Proposed High Fidelity Hybrid HiL Simulator

From the analysis in Section 2 we know the incapability for the processor-based HiL to calculate and output the stator currents between the time grids causes the HiL delay. By investigating the VSI-motor state space equation (5) we see that the derivatives of the system state variable is composed of two parts: the self interaction of system state variables which is not associated with inverter switching function; the system input vector that is associated with inverter switching function that causes the ITS problem. Therefore it is convenient to let the FPGA calculate the part of derivative associated with the fast changing switching function and consider the part derivative caused by self interaction of state variables as constant between processor time grids. If the processor simulation time step is chosen to be relatively small (25 µs), this assumption can be justified since it is only a small fraction of the time constant (several ten milliseconds) that determines the dynamics of state variable self interaction. If the FPGA simulation time step is selected to be very small (50 ns), high simulation fidelity comparable with that of a pure FPGA simulation can be achieved as is shown in Section 5. The switching function of the VSI is stored on the FPGA RAM memory and can be initiated at the start of the HiL simulation and reconfigured by the user. The state variables affected by the switching function, in our case the stator currents, are calculated by numerical accumulator using explicit Euler method on the FPGA and after inverse Clark transformation outputted via the D/A converter on the FPGA board to the drive controller, thus almost eliminates the HiL delay discussed in Section 2. The principle of proposed hybrid solution is illustrated in Fig. 5.

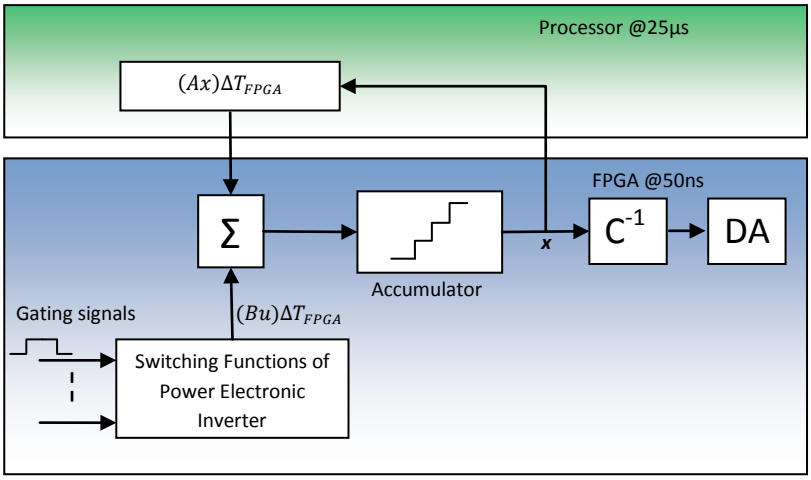

Fig.5. Principle of hybrid solution

5. Closed-Loop Experiment with Three-Phase Induction Motor Drive Controller and Comparison with Pure FPGA Solution

To validate the proposed hybrid solution, closed-loop experiments with a practical deployed induction motor drive controller are conducted. The controller hardware is based on a dual processor structure with PowerPC processor and digital signal processor (DSP). The controller software is based on rotor field oriented cascaded speed/current control and SPWM modulation. Regular sampling technique is used to synchronize the measurement and control of stator currents. The detailed explanation of this control algorithm can be found in [12].

A pure FPGA-based HiL simulator running at 50 ns and a HiL simulator implementing the proposed hybrid solution are connected to the same drive controller respectively for comparison. The drive controller was originally used to control a squirrel cage induction machine with rated power comparable to an urban metro traction motor, its parameters are listed in table 1. For the purpose of test both HiL simulators are configured with the same parameters.

Table 1: Stator side related parameters of induction motor used in the simulation

Stator resistance [Ω]	0.0143
Rotor resistance [Ω]	0.0306
Stator leakage inductance [mH]	0.324
Rotor leakage inductance [mH]	0.0853
Mutual inductance [mH]	6.1025

In the experiment, the controller works in speed control mode, the speed command is set to 1000 min^{-1}. To enhance the advantage gained by proposed hybrid solution, the carrier frequency of the SPWM modulation is set to 9.09 kHz.

Both HiL solutions are implemented on identical FPGA devices (xc5vsx95t of the company Xilinx Inc.). Table 2 gives an overview to FPGA resource consumption by hybrid and pure FPGA HiL simulator, respectively. Since the most critical resources for FPGA devices are slice logic and DSP blocks, only these two items are listed here.

Table 2: Comparison of critical FPGA resource

Critical resources	Hybrid HiL consumption	pure FPGA HiL consumption
Slice logic	9%	19%
DSP48E	0%	26%

From Table 2 it is clear that due to the reduction of multiplication and division, the usage of DSP blocks (DSP48E) is completely spared by hybrid HiL, whereas the relative large consumption of this resource by pure FPGA solution would limit its model expansion potential.

The HiL responses are recorded as feedback signals by the controller at 110 µs sample rate and transmitted via optical cable to PC. Fig. 6 compares the responses at 1000 min^{-1} in sudden load torque change from 100 Nm to 500 Nm between pure FPGA and hybrid simulators respectively. The relative speed error of less than one percent clearly demonstrates that the proposed hybrid HiL simulator displays almost the same dynamic behavior in the Closed-Loop as the pure FPGA HiL simulator. A closed-up view of motor phase currents of both HiL simulators before and after the load change further supports this point.

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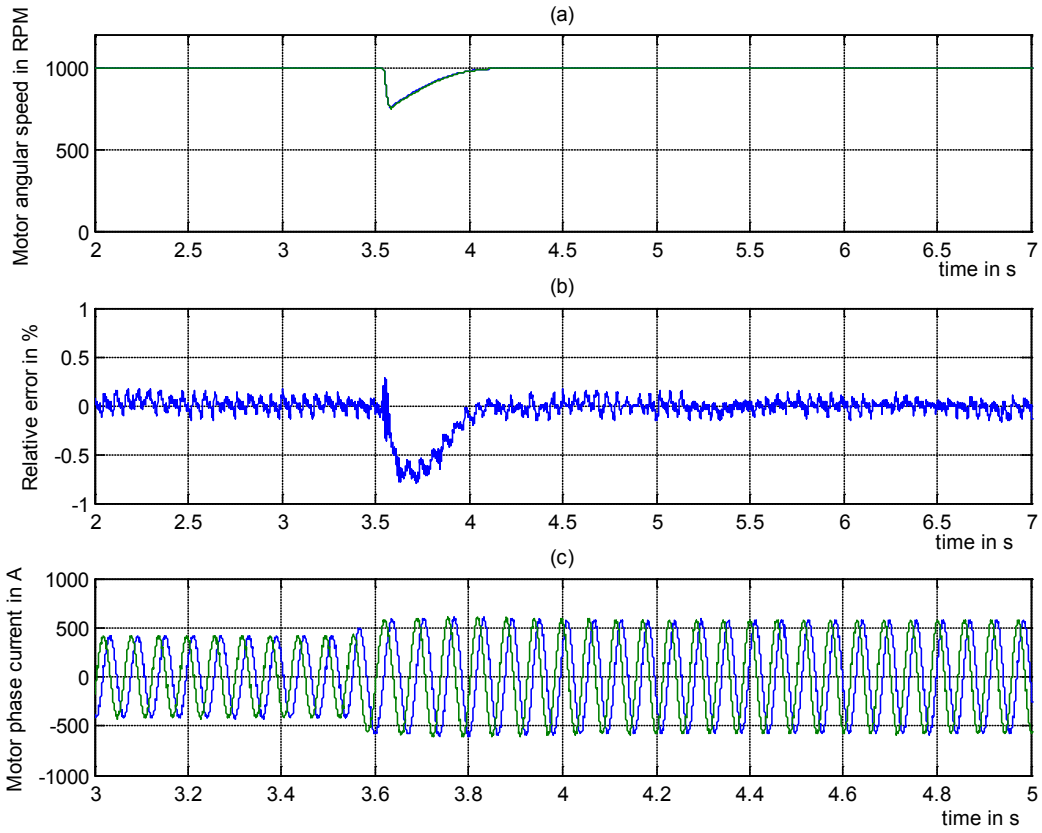

Fig. 6. Transient comparison between hybrid and pure FPGA HiL simulation under sudden load torque change from 100 Nm to 500 Nm: (a) the angular speed response, where the blue line hybrid HiL simulation results whereas the green line the pure FPGA HiL simulation results; (b) the percentage of angular speed relative error between hybrid and pure FPGA HiL simulation, absolute error related to 1000 min^{-1}; (c) Closed-up view of motor phase currents comparison during load change transients, where the blue line hybrid HiL simulation results whereas the green line the pure FPGA HiL simulation results

6. Conclusion

In this paper, we have analyzed the challenges of real time digital simulation of power electronic and drive systems as applied on railway vehicles, especially the extra delay that is introduced by the HiL. We presented a novel hybrid HiL simulator to combine the advantages of both processor HiL simulators and pure FPGA HiL simulators and meanwhile overcoming their drawbacks. Comparison experiments with an three-phase induction motor drive controller show that the proposed hybrid HiL simulator is capable to reduce the HiL delay and achieve the precision of a pure FPGA HiL simulator meanwhile reduce the FPGA resource consumption compared with pure FPGA HiL simulator.

7 Acknowledgment

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8. Literature

[1] Scheiben, E.: Antriebssoftware für Schienenfahrzeuge im Stresstest. dSPACE User Conference 2010, Paderborn, Germany, 2010

[2] Keller, T, Scheiben, E, Terwiesch, P.: Digital Real-Time Hardware-in-the-Loop Simulation for Rail Vehicles: A case study. European Conference on Power Electronics, 1997

[3] Mahmoud, M.; Reza, I.: FPGA Implementation of the Power Electronic Converter model for Real-Time Simulation of Electromagnetic Transients, IEEE Transaction On Power Delivery, Vol.25, No.2, April 2010

[4] Christian, D.: Accurate Simulation of a 6 Pulse Inverter with Real Time Event Compensation in ARTEMIS. Electrimacs 2002, August 18-21

[5] Faruque, M.; Venkata, D.; Wilsun, X.: Algorithms for the Accounting of Multiple Switching Events in Digital Simulation of Power Electronic Systems. IEEE Transactions On Power Delivery, Vol 20, No.2, April 2005

[6] dSPACE GmbH.: User's Manual of Electric Motor Simulation Board DS5202 EMH, 2009

[7] Christian, D.; Jean. B.; Simon; A.; Vincent, L.: FPGA-Based Real-Time Simulation of Finite-Element Analysis Permanent Magnet Synchronous Machine Drives. IEEE Power Electronics Specialists Conference, PESC 2007

[8] Boecker, J.: Leistungselektronik. Lecture Notes, University of Paderborn, Paderborn, Germany, 2010

[9] Steimel, A.: Elektrische Triebfahrzeuge und ihre Energieversorgung – Grundlagen und Praxis. 2.Auflage., Oldenbourg Industrieverlag, Germany 2006

[10] Franzen, F; Nelles,D.; Tuttas, C.: Anschauliche Darstellung einfacher Integrationsalgorithmen. etzArchiv 10 (1988) no.8

[11] Boecker, J.: Discrete-Time Model of an Induction Motor. ETEP Vol.1, No.2, March/April 1991

[12] Boecker, J.: Geregelte Drehstromantriebe. Lecture Notes, University of Paderborn, Paderborn, Germany, 2011

[13] Quang, P.; Dittrich, A.: Vector Control of Three-Phase AC Machines: System Development in the Practice, 1st Edition, Springer Verlag, Berlin, 2008