Analysis and Design of Improved Isolated Full-Bridge Bi-Directional DC-DC Converter

Rongyuan Li, Andreas Pottharst, Norbert Fröhleke, Joachim Böcker
Institute of Power Electronics and Electrical Drives
University of Paderborn, Germany

***Abstract*—A novel isolated full-bridge DC-DC converter with bi-directional power flow is proposed in this paper. By adding auxiliary active clamping circuits to both bridges, zero-voltage and zero-current-switching are achieved to improve the performance of the bi-directional PWM converter. The switches are controlled by phase shifted PWM signals with a variable duty cycle. The principle of operation is analyzed and simulated. Experimental results of a 3 kW 50 kHz prototype are presented.**

I. INTRODUCTION

In hybrid electric vehicles and rail guided shuttles, electric power distribution systems operate at different voltage levels due to the availability of storage devices. Electric motors for traction and fuel cells are connected by a high voltage bus, while batteries and ultracapacitors are mostly connected by a low voltage bus. Bi-directional converters controlling the energy flow between these energy sources are thus required. Therefore high power full-bridge bi-directional converters have become an important research topic during recent years [1] [2].

The current-fed full-bridge and the voltage-fed full-bridge are the essential structure parts. Two voltage-fed full-bridges are the subcircuits of the Dual Active Bridge (DAB), which contain less components as the circuit under investigation and ZVS is achieved in the resonant range [3]. The disadvantage of this circuit is that the performance of the converter is largely determined by the parameters of the transformer, because the leakage inductance is used for storing and transferring energy. Additionally, the freewheeling currents increase the losses and reduce the effective duty cycle.

An alternative topology is shown in Fig. 1, consisting of a current-fed full-bridge at the lower voltage side and a voltage-fed bridge at the high voltage side. Inductor L performs the output filtering, when the energy flows from high voltage bus to batteries or ultracapacitors, described as BUCK mode; alternatively it works as boost inductor, when energy is provided by the storage element, which is BOOST mode. Advantages of this topology are: The freewheeling current is small, and the leakage inductance is only used as energy transferring element, thereby a largely simplified transformer results when compared with DAB. But the transformer leakage inductance may still cause high voltage transients across the bridge switches due to the current feeding nature, which increases the switching stress and decreases the reliability.

The simplest remedy is by employing a RCD snubber to clamp the voltage, but a lower efficiency is the resulting drawback. An "active commutation" control principle was published in [4] in order to control the current of leakage inductance; however clamping circuits are additionally requested. A buck converter or a flyback converter is employed in industrial use in order to replace RCD snubber, but the still needed clamping circuits presented in [8] and [10] are too complex. Considering the boost operational mode, the leakage inductance of the transformer should be very small. The energy stored in the leakage inductance is not sufficient to realize ZVS for the lagging leg. A simple active clamping circuit is employed in [5] and [11], which suits for bi-directional converters [6]. Unluckily, the resonant current increases the current stress of switches largely.

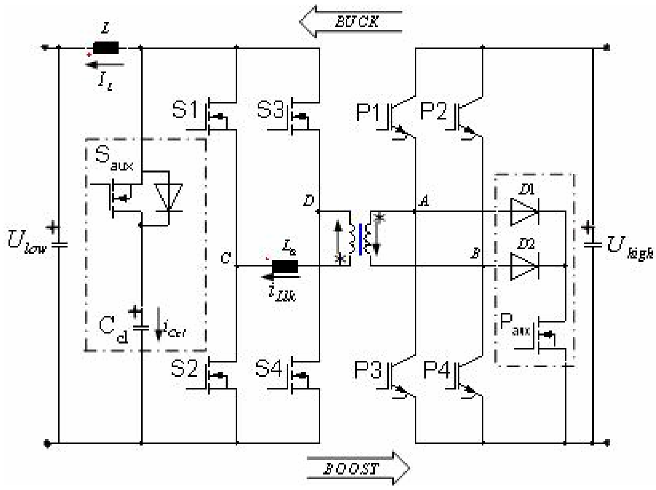


Fig. 1 Proposed bidirectional converter

In this contribution an improved full-bridge converter shown in Fig.1 is proposed, where by means of a simple auxiliary circuit at the voltage side, cooperating with an active clamping circuit consisting of S_{aux} and C_{cl} on the current-fed side ZVZCS is achieved for voltage-fed side switches and ZVS for current-fed side switches. Furthermore by delaying the turn-off time of switches S1 and S3, and by adding a simple auxiliary circuit consisting of P_{aux} and two diodes at the voltage side the switches at current-fed side are operated by ZVZCS. Moreover, the resonant current between the clamping capacitor and leakage inductance is limited, thereby improving the converter efficiency significantly.

II. PRINCIPLE OF CIRCUIT OPERATION

Operation diagrams are shown in Fig. 2 and Fig. 3. The phase shifted PWM control serves as control for both modes. In boost mode, switches S1~S4 are controlled, and the diodes of switches P1~P4 are used as rectifier. Contrary in buck mode, switches P1~P4 are controlled, and the diodes of switches S1~S4 operate as rectifier. To simplify the steady-state analysis, several assumptions are made as follows:

(1) All components are ideal. The transformer is treated as an ideal transformer and a leakage inductance.

(2) Inductor L is large enough to keep the current I_L constant during a switch period in both working modes.

a. Buck converter mode of operation.

The leading-leg switches P1 and P3 are operated at ZVS and the lagging-leg switches P2 and P4 are operated at ZCS by using auxiliary switch and clamping capacitor. This is appropriate for converters, in which the leakage inductance of the transformer is very small $(L_{lk} < 1\mu\text{H})$. The detailed operation analyses have been presented in [6] and other papers.

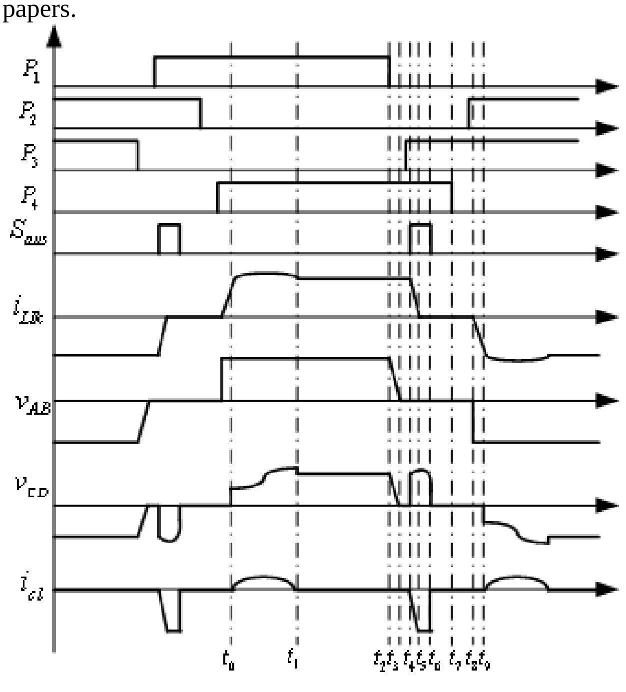


Fig. 2 Operation diagram of buck mode.

b. Boost converter mode of operation.

As above explanation by cooperating auxiliary switches S_{aux} and P_{aux} shown in Fig. 1, the lower-leg switches S2 and S4 are operated at ZVS, and the upper-leg switches S1 and S3 are operated at ZCS, moreover the voltage stress of the switches are limited.

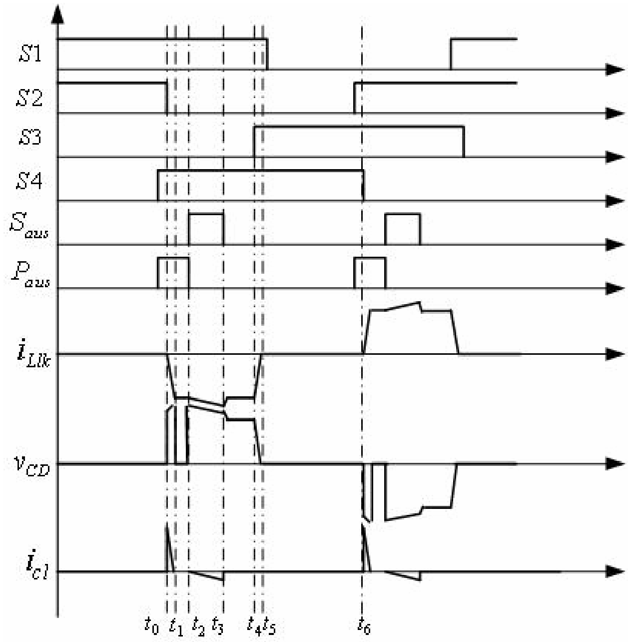


Fig. 3 Operation diagram of boost mode.

The operation stages are shown in Fig. 4.

Mode 0 [$t < t_0$]: S1, S2 are conducted, so boost inductor L is charged, and the transformer is shorted. S4 and P_{aux} are turned on, because the bridge is shorted also by S1 and S2, S4 is turned on at ZVS.

Mode 1 [$t_0 < t < t_1$]: At t_0, S2 is turned off. The parallel diode of switch S_{aux} conducts by freewheeling of boost current I_L, C_{cl} and L_{lk} resonate. At t_1, i_{Ccl} is zero and i_{Llk} equals I_L.

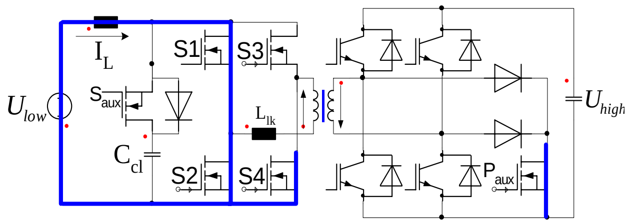
Mode 2 [$t_1 < t < t_2$]: After t_1, P_{aux} is still turned on, i_{Llk} is freewheeling.

Mode 3 [$t_2 < t < t_3$]: At t_2, P_{aux} is turned off, S_{aux} is turned on. The energy is delivered to the voltage-fed side. In this stage the clamping capacitor C_{cl} is discharged, the snubbed energy is then delivered to voltage-fed side.

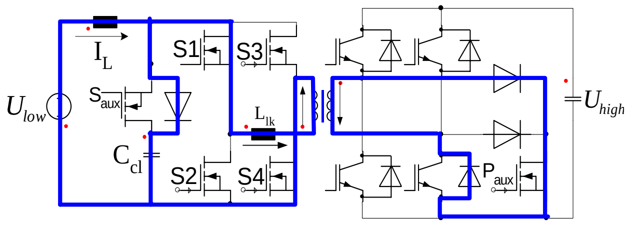
Mode 4 [$t_3 < t < t_4$]: At t_3, S_{aux} is off. The energy is still delivered to the voltage-fed side. And in this mode, $i_{Llk} = I_L$.

Mode 5 [$t_4 < t < t_5$]: At t_4, S3 is turned on by ZCS due to the leakage inductance. After S3 turned on, i_{Llk} is decreased to zero by the reflected voltage from voltage-fed side.

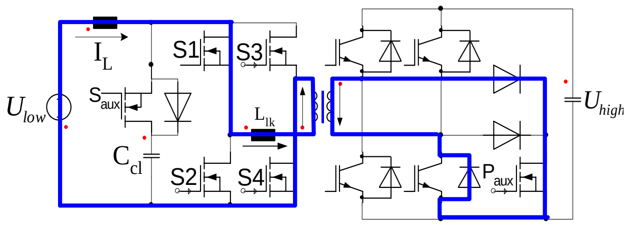
Mode 6 [$t_5 < t < t_6$]: After $i_{Llk} = 0$, S1 can be turned off by ZCS. The boost inductor L is charged. At t_6, the next half period begins.



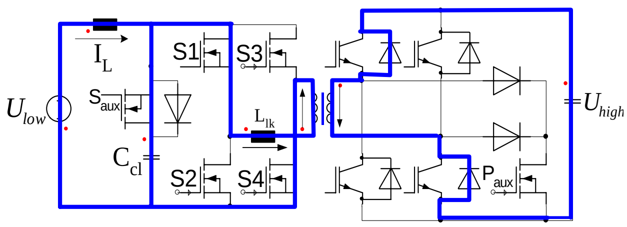
(a) Mode 0 [$t < t_0$]



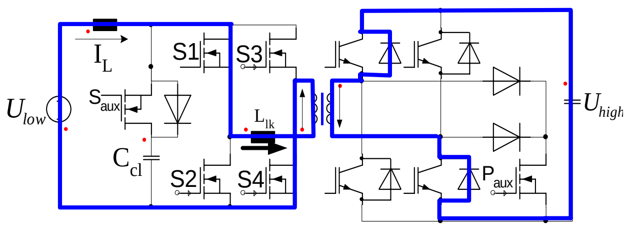
(b) Mode 1 [$t_0 < t < t_1$]



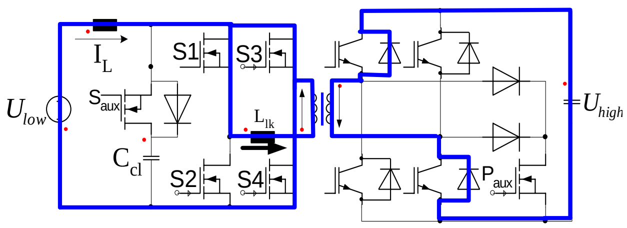
(c) Mode 2 [$t_1 < t < t_2$]



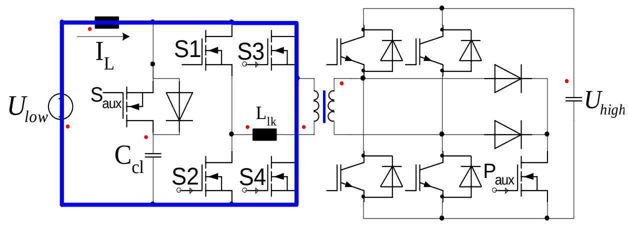
(d) Mode 3 [$t_2 < t < t_3$]



(e) Mode 4 [$t_3 < t < t_4$]



(f) Mode 5 [$t_4 < t < t_5$]



(g) Mode 6 [$t_5 < t < t_6$]

Fig.4 Operation stages of boost mode.

III. DESIGN CONSIDERATIONS

a. Soft switching condition

(1) Current-fed side

The lower-leg switches S2 and S4 are turned on at ZVS in any load condition, because the current-fed bridge is shorted before S2 and S4 are turn on.

The delay between the upper-leg current-fed switches should be longer than interval [$t_5 < t < t_6$].

The minimum delay time is:

$$T_{d\,\min\_S1S2} = L_{lk}\, I_L / V_{CD} \tag{1}$$

(2) Voltage-fed side

The dead time for leading-leg switches are determined by the load and the input voltage, the minimum dead time should be as long as the capacitor resonance time:

$$T_{d\,\min\_P1P3} = (C_{P1} + C_{P3}) U_{high} / n I_L \tag{2}$$

For the lagging-leg switches ZCS operation is determined at the maximum duty cycle. Before turned-on the lagging-leg switches, the leakage inductance current should be zero. So the reserved time is:

$$T_{r\,\min\_P2P4} = L_{lk}\, I_L / V_{CL} \tag{3}$$

(3) Clamping capacitor

Due to discharging of the leakage inductance the energy stored in the clamping capacitor should be satisfied with the maximum required energy, so

$$C_{cl} \geq L_{lk} I_L^{\,2} / V_{CL}^{\,2} \tag{4}$$

b. Reduction of the snubbed energy

In the interval [$t_0 < t < t_1$], the high transient voltage occurs inevitably in boost mode, which could be snubbed by the clamping branch (S_{aux}, C_{cl}). The snubbed energy of C_{cl} is transferred to the voltage-fed side via switches S1~S4, hence a minor increase of current result for switches. The auxiliary switch P_{aux} is also employed to reduce the snubbed energy; subsequently, the current stress can also be reduced.

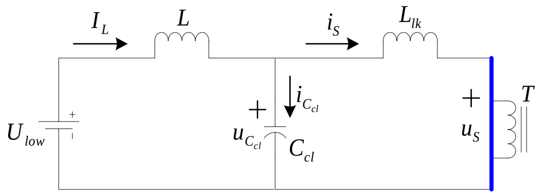


Fig.5 Equivalent current of boost mode interval t0~t1

In the mode 1 [$t_0 < t < t_1$], the current i_S and $i_{C_{cl}}$ can be formulated as follow:

$$
\begin{aligned}
i_{C_{cl}} &= I_L \cos(\omega_0 t) - \sqrt{C_{cl}/L_{lk}}\,(U_{C_{cl}0} - U_s)\sin(\omega_0 t) \\
i_S &= I_L - i_{C_{cl}} \qquad (5) \\
\text{With} \quad \omega_0 &= 1\big/\sqrt{C_{cl} L_{lk}}
\end{aligned}
$$

When P_{aux} is conducting, the transformer is clamped. Hence the voltage V_s equals zero, the leakage inductance current i_S increases sharply, and the clamping capacitor current decreases quickly. The energy flowing through clamping circuit is reduced and can be expressed as :

$$
\begin{aligned}
W_{C_{cl}} &= \frac{2U_{C_{cl}0}}{T_s \omega_0}\left(I_L \sin(\omega_0 t_r) + \sqrt{C_{cl}/L_{lk}}\,U_{C_{cl}0}(\cos(\omega_0 t_r) - 1)\right) \qquad (6) \\
t_r &= \frac{1}{\omega_0}\arccos\left(\frac{\sqrt{C_{cl}}\,U_{C_{cl}0}}{\sqrt{C_{cl} U_{C_{cl}0}{}^2 + L_{lk} I_L{}^2}}\right)
\end{aligned}
$$

As the commutation interval is reduced, the dynamic response and the efficiency of converter will be increased.

(4) Control strategy

The complete control strategy block diagram is shown in Fig. 6, which is integrated with the control for boost and buck mode operation together, therefore the cost for controlling section is reduced.

The voltage control and average current control are used here to control the energy flow and to improve the converter dynamic behavior and stability. The current control loop of boost mode and buck mode are implemented by using analog current compensator and PWM modulator, while the voltage control loop is realized using a DSP controller.

The DC-bus voltage and the voltage of the energy storage element are sampled by the DSP controller as voltage feedback. According to the working mode, the situation of the load and energy storage element, the current references are given by the DSP to the current compensators. The current of inductor L is employed as current feedback. There are two phase shift PWM IC UCC3895 used as PWM modulator to generate the gate drive signals.

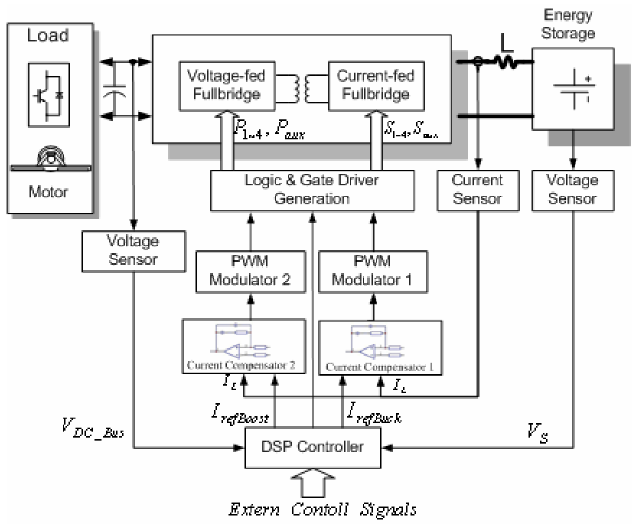


Fig. 6 Control strategy for bidirectional converter

The gate drive signals of the auxiliary switches shown in Fig. 2 and Fig. 3 are generated by a CPLD, which is employed also to monitor the fault signals of the converter and to perform the protection schemes.

IV. SIMULATION ANALYSIS

To verify the theoretical analysis of the proposed topology, simulation models are built in SIMPLORER using the following design specification: $U_{Low} = 40\text{V}$, $U_{High} = 650\text{V}$, $L_{lk} = 0.5\mu\text{H}$, $L = 23\mu\text{H}$, $C_{Cl} = 2\mu\text{H}$, and the switching frequency $f_S = 50\text{kHz}$.

Simulation results of buck mode are shown in Fig. 7, and Fig. 8 displays the boost mode simulation results. The transformer primary side voltage u_{AB} and secondary side voltage u_{CD} , leakage inductance current i_{Llk} , clamping capacitor current i_{Ccl} and voltage u_{Ccl} are displayed.

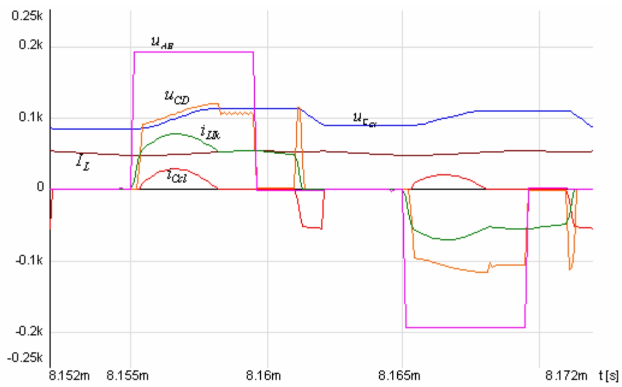


Fig. 7 Simulation results of buck mode.

In Fig. 7, the clamping capacitor C_{Cl} forces current i_{Llk} to zero, thus the legging leg switches could work at ZCS.

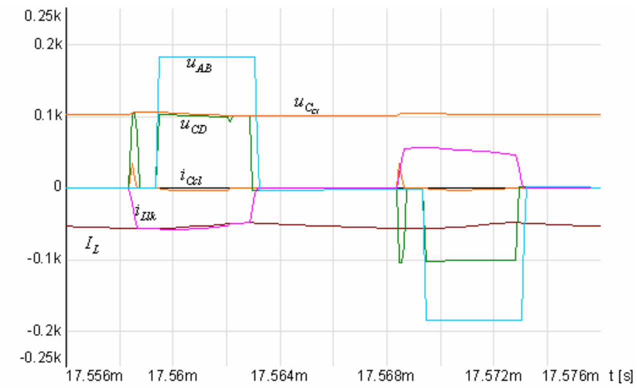


Fig. 8 Simulation results of boost mode.

From Fig. 8 we see that the simulation results agree well with the theoretical waveforms of Fig.3. With the functions of the auxiliary switch P_{aux} the resonant current between clamping capacitor C_{Cl} and leakage inductance L_{lk} is reduced, thus the current stress of switches are also reduced.

V. EXPERIMENTAL RESULTS

A 3kW experimental prototype is built to verify the operation principle of the proposed converter. A supercapacitor module working at the low voltage side is employed as energy storage element, whose voltage range is 20~42V. The high voltage range is 500~750V. The parameters of circuit are listed as follow:

TABLE I

Component		Value
$P_1 \sim P_4$	IGBT	IXGH 15N120CD1
$D_{P1} \sim D_{P4}$	antiparallel diodes of IGBT	DSEI 30-12A
P_{aux}	MOSFET	IXFX 24N100
$S_1 \sim S_4$	MOSFET	IXFH 88N20Q
S_{aux}	MOSFET	IXFH 88N20Q
C_{cl}	snubber capacitor	2.4μF
n	transformer turns ratio	3 : 24
L_{lk}	leakage inductance	0.5μH

The experimental waveforms of the input inductor current, the current-fed side transformer current and the voltage across the transformer at boost mode are shown in Fig. 9. The test waveforms of the clamping circuit are shown in Fig. 10. The output power is 500W in this test and the measured efficiency is 90.3%.

From the experiments, it can be seen that the voltage peaks caused by transformer leakage inductance are reduced by the clamping circuit.

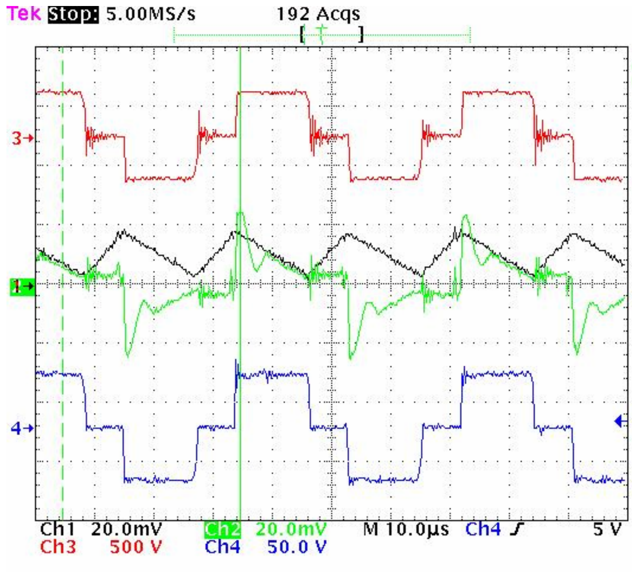


Fig. 9 Boost mode tests.

Ch1: Inductor current i_L (10A/div).

Ch2: Current-fed side transformer current i_{Llk} (10A/div).

Ch3: V_{AB}.

Ch4: V_{CD}.

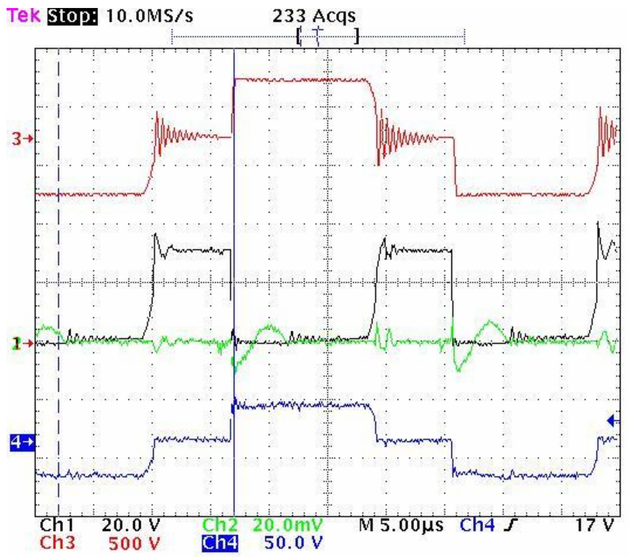


Fig. 10 Clamping circuit test at boost mode.

Ch1: Voltage of clamping switch Saux.

Ch2: Current of clamping capacitor $i_{C_{cl}}$ (5A/div).

Ch3: V_{AB}.

Ch4: V_{CD}.

At the same time, the current stress of the current-fed switches are decreased. The resonances of V_{AB} are mainly caused by the leakage inductance and the parallel capacitors of the voltage-fed switches.

V. CONCLUSION

In this paper, a novel isolated full-bridge bi-directional DC-DC converter using phase shifted PWM control is presented. By using respective clamp circuits at current-fed and voltage-fed side, the voltage transient spikes across the circuit-fed bridge are limited, and all switches are operated at soft switching. The operating principles and design considerations are discussed and verified by simulations and experiment. The magnetic elements are need to be optimized and the detailed treatment of the average model derivation and closed loop control will follow in future publications.

ACKNOWLEDGEMENTS

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