Active Common-Mode Voltage Cancellation for Three-Phase PWM Rectifier/Inverter Systems based on a New Topology

P. Ide, F. Schafmeister, N. Froehleke

Institute for Power Electronics and Electrical Drives[1]
University of Paderborn, FB-14 LEA
Pohlweg 47-49, 33098 Paderborn, Germany
Phone & Fax: +49 5251 60 3157
e-mail: Peter.Ide@epost.de

Abstract-**After giving a summary of investigated passive and active schemes to mitigate common mode problems a modeling approach for the common mode voltage (CM voltage) is presented for three-level rectifiers. A novel Active Common-mode Voltage Cancellation (ACC) scheme is proposed, utilizing the reconstructed CM voltage to derive a simpler driving scheme as presented by previous contributions. The ACC scheme function based on switched mode operation is explained, modeling and design of the power circuitry including a 5-winding transformer is outlined and simulation results prove its viability and effectiveness in eliminating CM voltage in a 3-phase / 3-level rectifier for telecom systems. A verification of the physical implemented circuitry is obtained from selected measured results on mentioned overall system**

I. Introduction

Three-phase high power factor switched mode rectifiers (PFC-SMR) are undergoing rapid development in recent years while more and more adjustable drive systems are fed by three-phase inverters. In contrary to single-phase and DC-systems all these systems act as common-mode voltage (CM voltage) sources. Typically this leads to high earth currents due to parasitic capacitive, conductive or magnetic coupling causing noise and EMI-problems, may reduce system reliability, degree of utilization and other problems outlined e.g. in [5] and [7].

Measures published solving these problems of three-phase systems are discussed in chapter II supplemented by an analysis about the generation of CM voltage, based on Three-Phase/Three-Level rectifiers, which is even more complex than for standard two-level systems. Measures to alleviate the negative impacts of common-mode noise presented to literature so far are discussed briefly, too.

In chapter III a new topology for Active Common Mode voltage cancellation (ACC) is introduced. The principle of operation, design guidelines and simulation results are presented. First measurement results gained on a prototype of the ACC-scheme operating in conjunction with a Three-Phase/Three-Level rectifier as shown in Fig. 1 are discussed. A short summary concludes this contribution.

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II. Common-Mode Voltages – Measures to Mitigate the Negative Effects

The generation of CM voltage as source of noise problems in Three-phase drive systems is well described in [7] as well as measures to attenuate this type of noise. Proper shielding and grounding as well as the mechanical design help to mitigate the noise problem, but nevertheless additional filter measures are still required. This means, common-mode chokes are inserted into motor leads or/and utility and signal leads. Similar problems are found in Three-Phase power systems, where due to power quality regulations switched mode rectifiers are installed (see [9]). The emergence of high-speed switching devices has on the one hand enabled the required increase in switching frequency for lower THD and higher power density designs but on the other hand the high dv/dt, di/dt ratings can cause a multitude of CM problems termed in [5] and [7].

A. Methods Presented to Literature

During last years different solutions to mitigate the problems caused by CM voltages by filtering or compensation have been presented to literature. In [2] different passive and one active solution(s) are compared. The active solution is designed to compensate the CM voltage, by adding the inverse CM voltage to the output voltages with the need of a fourth inverter leg. According to [2] this method shows no visible progress in comparison to

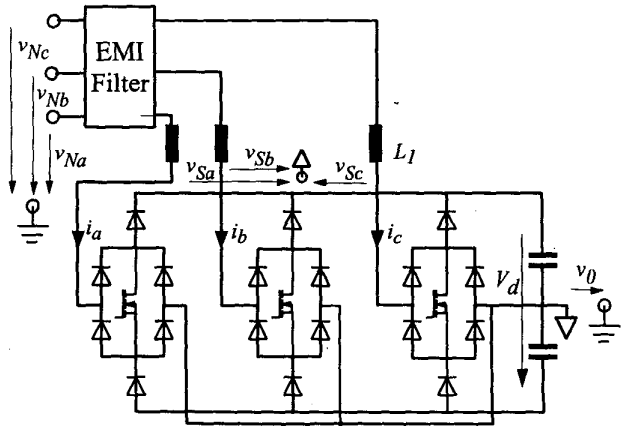

Fig. 1: Three-level rectifier presented in [11] (3-level SMR)

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passive methods, one reason might be the very rough image of the reconstructed inverse CM voltage leading only to a quasi-compensation. In [1] an alternative modulation scheme is suggested, aiming on a reduction of CM noise. The drawbacks of this method are higher current ripple and, what is even worse, the available output voltage $\hat{V}_S$ is reduced to $\frac{2}{3\sqrt{3}}V_d$, while the upper limit is $\hat{V}_{S,\max} = 1/\sqrt{3}V_d$ at standard space-vector (SV) modulation.

A four leg converter, similar to that in [2] and an adapted modulation scheme are presented in [6]. Applying this modulation scheme is accompanied with some drawbacks, i. e. the current ripple will be higher and current shaping is deteriorated or the available output voltage declines to $\sqrt{3}/4V_d$. However, this modulation scheme and the one proposed in [1] cannot be applied to three-level rectifiers as shown in Fig. 1 or the similar one presented in [12], because the available switching states depend on the signs of the phase currents. But, nevertheless, this method leads to a much better approximation of the CM voltage, thus a significant reduction of CM noise results. In [3] a seven-leg inverter is proposed to compensate the CM voltages, but due to the high number of parts this does not seem to be a practical solution. In [10] a PWM strategy for 3-level inverter is proposed, which resembles the one used for the 3-level SMR anyhow.

Contrary to discussed schemes the solution presented in [5] is based on a fourth winding added to the CM choke, thus it is operated as a transformer. This fourth winding is fed by a linear amplifier, which generates the inverse CM voltage. This method seems to be effective and useful, because no drawback for the design of inverters results. But the linear amplifier generates a high power dissipation and the need of a high magnetizing inductance of the CM transformer leads to a bulky device. The principle of operation of an active compensator proposed in [8] is based again on a four winding CM transformer. But this fourth winding is fed by a switched–mode four level half-bridge inverter, build up with a series arrangement of 6 semiconductors. The parts count and the complexity to drive all these semiconductors is quite high and balancing the series arrangement of the six capacitors is unsolved. The Three-Phase/Three-Level rectifier according to Fig. 1 which proved as an optimum topology e.g. for feeding telecommunication systems in conjunction with CM problems is focused solely in [4]. The proposed simple method is most suitable for rectifier systems. The circulating reactive power is regarded as disadvantage, causing additional losses, especially due to higher ripple currents of inductors.

B. Modeling of CM voltages

The modeling of CM voltage of three-level systems is performed similar to two-level systems (see [7]), Thus only differences should be discussed here in detail. Generally CM voltage can be equated by a zero-component to be calculated with (1), where the pulsating input voltages v_s of the rectifier are referred to the centerpoint of the DC-link voltage as depicted in Fig. 1.

$$v_0 = \sum_{k\in a,b,c} v_{s,k} \tag{1}$$

Without filtering this voltage v_0 can be measured between the mains star point and the output voltage centerpoint of the three-level rectifier. In three-level systems five different levels of this voltage have to be distinguished in total, while only 4 levels of the CM voltage are found in 2-level systems. The measured waveforms in Fig. 2 and Fig. 3 show the CM voltage at a three-level SMR. In addition to the four levels visible in Fig. 2 zero has to be taken into account. A more detailed analysis shows, that for each combination of input current signs the CM voltage can be described by four different levels visible in Fig. 3 (see Table I).

The behavior of semiconductor stage in conjunction with the output capacitors of typical three phase systems can be described by pulsating voltage sources. The gray shaded area in Fig. 4 represents this part by five voltage sources. The input voltages can be divided into three differential mode (DM) voltage sources v_{DM}, representing a symmetric

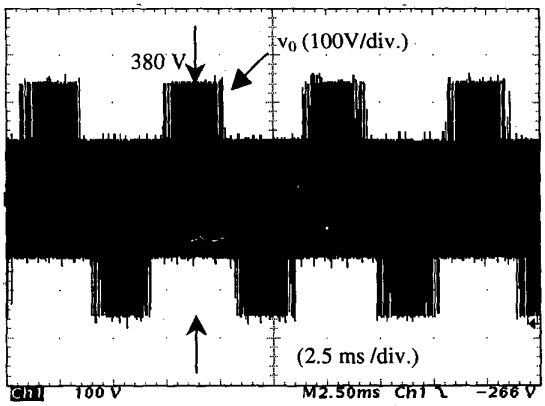

Fig. 2: Measured CM-voltage on a 3-level SMR (Line cycle)

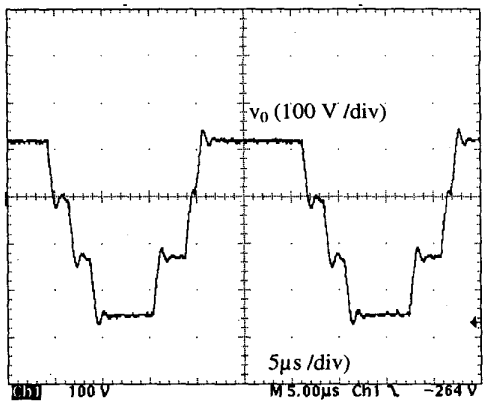

Fig. 3: Zoomed Measured CM voltage on a 3-level SMR (switching cycle)

TABLE I

OVERVIEW OF ALL SWITCHING STATES AND SIGNS OF INPUT CURRENTS, WHICH DETERMINE THE CM VOLTAGE OUT OF FIVE LEVELS

switching states	$i_a>0$ $i_b<0$ $i_c<0$	$i_a>0$ $i_b>0$ $i_c<0$	$i_a<0$ $i_b>0$ $i_c<0$	$i_a<0$ $i_b>0$ $i_c>0$	$i_a<0$ $i_b<0$ $i_c>0$	$i_a>0$ $i_b<0$ $i_c>0$	v_0/V_d
		++0		0++		+0+	+⅓
		++-		-++		+-+	+⅙
	+00		0+0		00+		+⅙
	+-0	+0-	0+-	-+0	-0+	0+-	+-0	0
	0-0		00-		-00		0-0	-⅙
	+--		-+-		--+			-⅙
	0--		-0-		--0			-⅓

voltage system and a CM voltage source. This CM voltage again can be split into low frequency components ($3f_N$) v_{0LF} and high frequency components v_{0HF}, respectively.

In Fig. 5 the low frequency rectangular components of the CM voltage with an amplitude of 1/12 V_d (different time scales) and the high frequency component (switching frequency f_s and harmonics, see also Fig. 6) are depicted. The shape of this HF component is very similar to CM voltages in standard two-level systems with its 4-level characteristic, while the amplitude is halved. Contrary to two-level systems typically the time intervals T_1 and T_4 are different, because the according states are used to balance the DC output voltages. At two-level systems these states belong to the zero-states <000> and <111>, which are typically selected of equal duration (refer to [7]).

III. A NEW TOPOLOGY FOR ACTIVE COMMON-MODE VOLTAGE CANCELLATION

A. *Principle of Operation*

The basic idea of ACC is to place controlled voltage sources in each phase inserting the inverse CM voltage. An equivalent schematic is given in Fig. 4, a more detailed schematic is presented in Fig. 10. Superimposing the original CM voltage and the inserted voltage v_2, which is realized by a transformer yields to no CM voltage for the overall system.

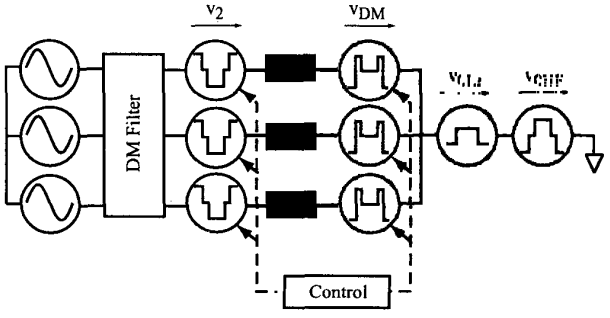

Fig. 4: Equivalent circuit of Three-Level rectifier and active compensation

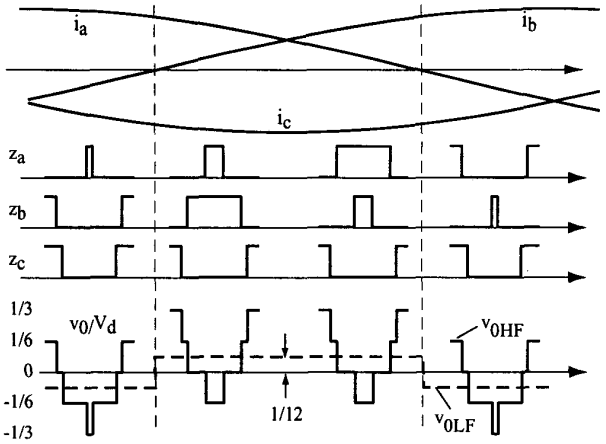

Fig. 5: Five different levels of the CM voltage have to be distinguished depending on the switching states and on the signs of input currents.

Hence, this method is similar to the principle presented in [5] for 2-level inverters. Latter transformer obtains three secondary windings, inserted into the ac leads; thus they carry the phase currents of the rectifier. Its primary side is fed by the inverse CM voltage. As mentioned above CM voltage of 3-phase converters contains low-frequency components according to the zero component applied to the modulation scheme. In order to reduce the size of the transformer only the high frequency components of the CM voltage should be compensated. Because most of the CM noise and earth currents are related to capacitive coupling or radiation the compensation of v_{0HF} is given formal attention, while low frequency components have negligible impact on EMI. Thus a four level signal $v_2 = -v_{0HF}$ according to Fig. 6 is to be generated. For loss minimization switched mode operation was selected, resembling to the idea presented in [8], where the primary side of the transformer is fed by a 7-level half-bridge converter. Here another solution is suggested. As depicted in Fig. 7 the reconstructed high-frequency voltage v_2 can be generated by superimposing two rectangular signals, where one signal v_{1a} has an amplitude of 1/6 V_d and alternates with switching frequency, while the other signal v_{1b} shows an amplitude of 1/12 V_d and three times the switching frequency of the rectifier. The rectangular input voltages can e.g. be generated by two half bridge legs.

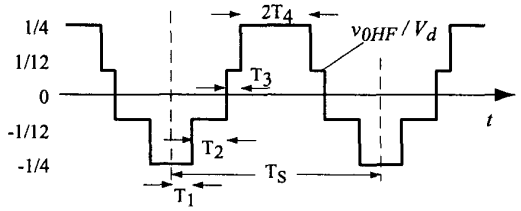

Fig. 6: HF component of CM voltages in detail resulting from Fig. 5, if varying of v_{0LF} is accounted for.

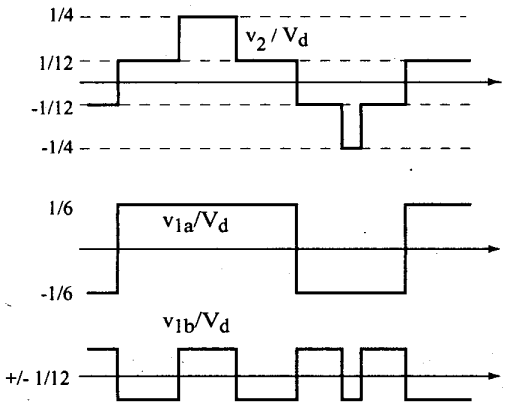

Fig. 7: Generation of the inverse CM voltage v_{0HF} by superimposing two rectangular signals v_{1a} and v_{1b}.

The amplitude of the rectangular voltages can be adjusted by different turns ratios. If the half bridges are fed by half of the output voltage $V_d/2$, then a turns ratio of $n_{1a}:n_{1b}:n_2 = 3:6:2$ is required. If the half bridges are fed by the full output voltage or if the rectangular voltage is generated by full bridge circuits, operated at half of the output voltage, then the turns ratio changes to $n_{1a}:n_{1b}:n_2 = 3:6:1$.

B. Design and Simulation results

Two possible arrangements of cores for this transformer were investigated. The first solution is based on E-cores, where one primary winding is placed on each return leg, while the secondary windings are placed on the center leg as depicted in Fig. 8. The output voltage v_2 inserted in the phase leads is defined by (2) using the addition of the flux in the return legs. Stray inductances are neglected.

$$v_{2a} = v_{2b} = v_{2c} = -\frac{n_2}{n_{1a}} v_{1a} - \frac{n_2}{n_{1b}} v_{1b} \qquad (2)$$

The currents in the secondary windings are the input currents of the converter, the instantaneous sum $i_{2\Sigma}$ of these currents should be almost zero. Nearly no power is transferred by the transformer. The currents in the primary windings can be calculated using (3) and (4). Λ_{1a} and Λ_{1b} specify the respective magnetic permeance of the return legs, while Λ_2 is the permeance of the center leg.

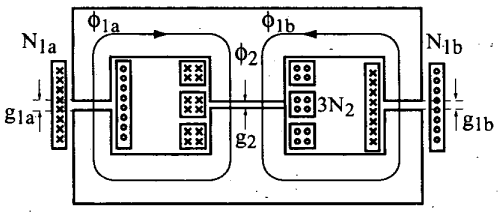

Fig. 8: Transformer to insert the inverse CM voltages with primary windings N_{1a}, N_{1b}, on each return leg and secondary windings (3 N_2) on center leg.

$$\frac{d}{dt}\begin{pmatrix} i_{1a} \\ i_{1b} \end{pmatrix} = \frac{1}{\Lambda_2}\begin{pmatrix} \frac{1+\gamma_a}{N_{1a}^2} & \frac{1}{N_{1a}N_{1b}} \\ \frac{1}{N_{1a}N_{1b}} & \frac{1+\gamma_b}{N_{1b}^2} \end{pmatrix} \cdot \begin{pmatrix} v_{1a} \\ v_{1b} \end{pmatrix} + \begin{pmatrix} \frac{n_2}{n_{1a}} \\ \frac{n_2}{n_{1b}} \end{pmatrix} \frac{d}{dt} i_{2\Sigma} \qquad (3)$$

$$\gamma_a = \frac{\Lambda_2}{\Lambda_{1a}} \approx 2\frac{g_{1a}}{g_2}, \quad \gamma_b = \frac{\Lambda_2}{\Lambda_{1b}} \approx 2\frac{g_{1b}}{g_2} \qquad (4)$$

Obviously also the primary windings are coupled, where the coupling coefficients are adjusted by varying the air-gaps. If half bridge or full-bridge topologies are feeding the transformer then current flow is independent of the feeding voltage. This means, coupling of the primary windings does not cause any drawbacks depart from more difficult system analysis. But even tiny air gaps in the return legs cause sufficient decoupling of the primaries. If $i_{2\Sigma}$ is neglected, the currents in the primary windings are magnetizing currents of the transformer. Without air gaps high magnetizing inductances and low reactive power levels can be achieved resulting in low power losses.

A second solution is based on two toroidal cores, where one primary winding is carried by each core and the three secondary windings are wrapped around both cores as depicted in Fig. 9. Total decoupling of both magnetic loops is achieved by this arrangement; thus no air gaps habe to be considered and higher inductances result accompanied with lower semiconductor losses. Again the secondary voltage can be calculated with (2), while the currents in the primaries are calculated separately.

Finally toroidal cores were selected for the prototype, because core materials with more suitable properties are available. Ferrite cores with high permeability rates or crystalline alloys are available only as toroidal cores optimized for CM chokes or filter applications. Crystalline alloys seem to be a good choice because of their high flux density rates resulting in smaller core dimensions.

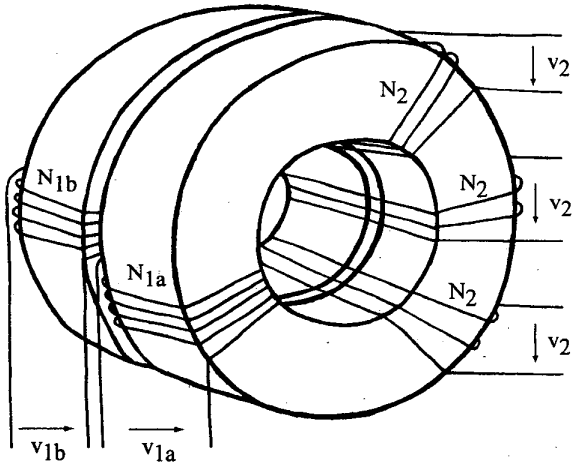

Fig. 9: Transformer to insert the inverse CM voltage based on two toroidal cores to achieve two independent magnetic loops, that induce the secondary voltage in the common windings.

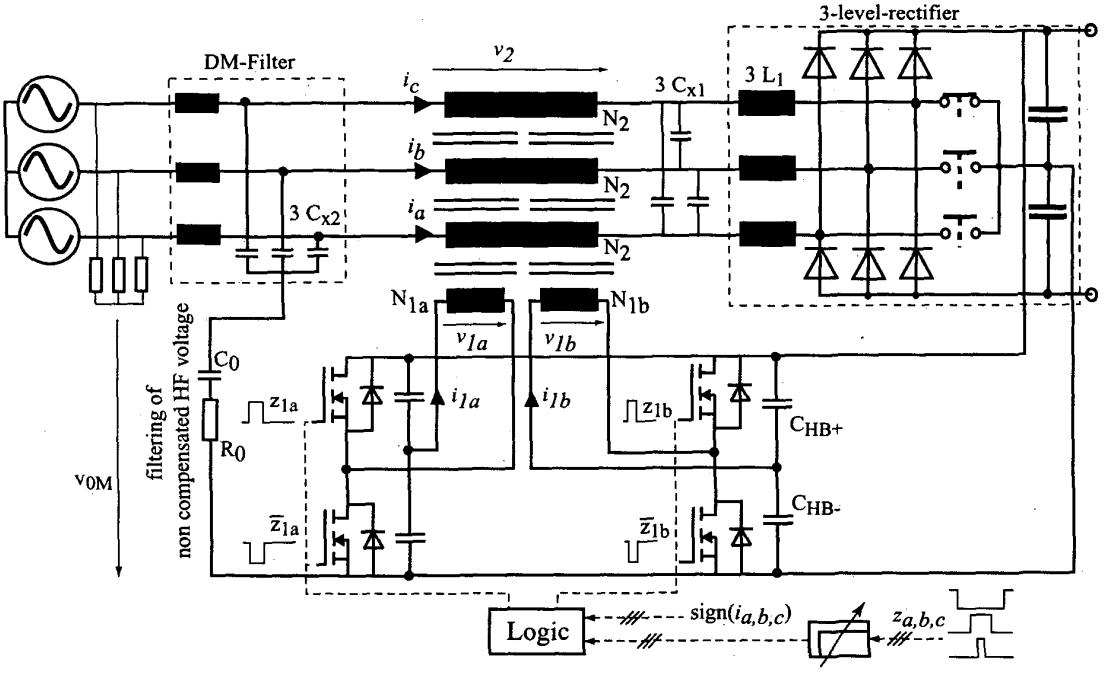

Fig. 10: Schematic of the proposed Active CM voltage cancellation circuit

Although the transferred power is very low, the volume of the transformer cannot be reduced proportionally. The number of turns of the secondary winding should be as low as possible to minimize the copper losses, while the number of turns of the primary windings should be high enough to minimize the core size. Flux and flux density respectively in the cores are determined by the applied voltseconds and the number of primary turns. Because of the fixed turns ratio a good compromise has to be found.

Another compromise is the selection of topology and input voltage. On the one hand, the input voltage should be as high as possible to achieve high turns ratios, on the other hand the feeding semiconductor arrangement should be as simple as possible to facilitate low cost solutions and switching behavior should be as ideal as possible. If the ACC is fed by $V_d/2$, then 500 V - MOSFETs can be selected instead of 1000 V types at typical applications ($V_d = 750\,V$). These perform much better due to their superior switching behavior, shorter delay time, better body diodes and even driving is more easy, especially, if the switching frequencies ($f_{sa} = f_s$, $f_{sb} = 3f_s$) of both bridges are considered. The size of the transformer is more or less independent of the amplitude of the feeding voltage, but input inductance as well as leakage inductance increase with input voltage. In order to keep the circuit as simple as possible and to avoid additional delay times resulting from isolating drivers the upper output voltage of the rectifier was selected to feed the ACC as depicted in Fig. 10. (The control scheme of the rectifier is referenced to the center tap potential.)

The half bridges are fed by complementary signals z_{1a} and z_{1b}, i.e. the voltage partitioning of the capacitors C_{HB+} and C_{HB-} varies according to the duty cycle similar to asymmetric half bridges. If C_{HB} are assumed to be voltage sources, than v_{1a} as well as v_{1b} contains low frequency components applied to the transformer. To assure, that the input voltages of the transformers are free of any low frequency component the dimension of the capacitors should be small according to (5) where the input impedance of the transformer is assumed to be the input inductance $L_{1a,b}$ and n is the harmonic order (related to mains period) of the low frequency common-mode voltage. Low frequency CM components higher than 5th order can be neglected, thus $n = 15$ lead to reasonable solutions. Hence, the fundamental frequency of CM voltage is equal to triple mains frequency.

$$C_{HB} << \frac{1}{(n\omega_N)^2 2L_{1a,b}} \tag{5}$$

The pulse pattern applied to the two half-bridges are determined by the sign of the input currents and the switching state of the rectifier represented by the gating

TABLE II
GENERATION OF PULSE-PATTERN WITH ACC LOGIC PART
FOR ($i_a > 0$, $i_b < 0$, $i_c < 0$)

z_a	z_b	z_c	state	v_0/V_d	v_2/V_d	z_{a1}	z_{b1}
0	0	0	(+--)	1/6	-1/12	1	0
1	0	0	(0--)	1/3	-1/4	1	1
0	1	0	(+0-)	0	1/12	0	1
0	0	1	(+-0)	0	1/12	0	1
1	1	0	(00-)	1/6	-1/12	1	0
1	0	1	(0-0)	1/6	-1/12	1	0
0	1	1	(+00)	-1/6	1/4	0	0
1	1	1	(000)	0	1/12	0	1

signals $z_{a,b,c}$. In Table II the combination between gating signals of rectifier and ACC is given for one set of input current signs. For other signs of input currents this can be expanded by swapping the indices in a cyclic way. The logic can be implemented easily by Gate Array Logic.

Simulation Results

This outlined scheme was proven and optimized step by step by simulation using *SABER*. The transformer model is based on an inductance matrix of a coupled inductor representation, furthermore delay times and some other parasitic effects are considered. Fig. 11 and Fig. 12 show simulation results to demonstrate the impact of the ACC on CM voltage. The CM voltage shows only low frequency components with peak values lower than 20 V (see zoomed v_0 in the upper part of Fig. 11.

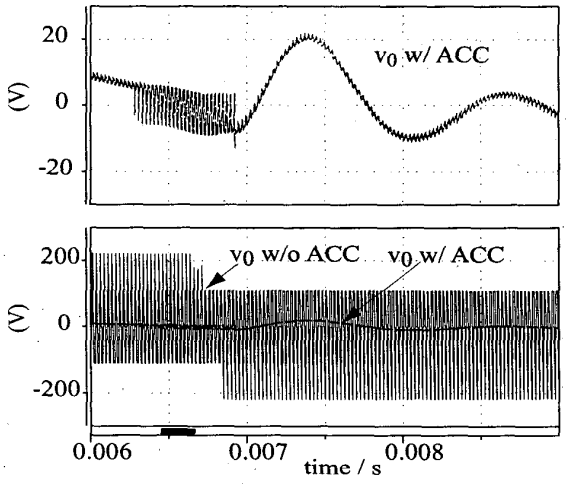

Fig. 11: CM voltage of the rectifier with and without active cancellation.

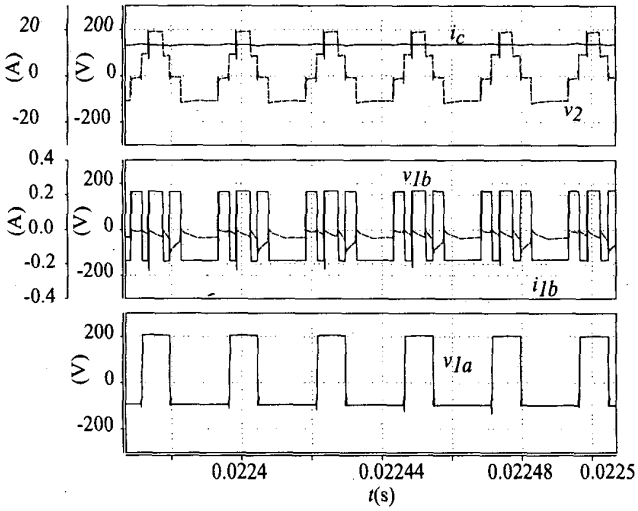

Fig. 12: Input and output voltage of the transformer as well as winding currents for a short interval of the mains period.

In the near of zero-crossings of the mains currents the high frequency components of CM voltage cannot be compensated completely due to special parasitic effects of this three-level rectifier, but even here the amplitude of the pulsating voltage is reduced by a factor of 15 (Fig. 11). In Fig. 12 typical voltage waveforms of the transformer windings are depicted. v_{1a} alternates with switching frequency of the rectifier, while the voltage v_{1b} can be described by four different time intervals according to Fig. 6. Phase current i_c loading one secondary winding shows no significant ripple, because a set of x-capacitors C_{x1} is inserted between rectifier and ACC. Current i_{1b} of one primary winding is basically the magnetizing current.

Improper Compensation

Due to parasitic effects a complete compensation of the CM voltage cannot be achieved. Basically two effects are distinguished. On one hand the amplitude of the compensating voltage v_2 is different from the amplitude of v_{0HF} resulting from voltage drops by damping resistors, leakage inductance or temporarily asymmetrical output voltage of the rectifier. This leads to a small spectral line of the resulting non compensated voltage at rectifiers switching frequency. On the other hand varying delay times lead to voltage spikes of the non compensated voltage. Typically delay times of the transistors of the rectifier and their associated isolating drivers are longer than the delay times of the ACC including its logic circuitry. These different delay times can partly be compensated by additional delaying of the pulsating signals $z_{a,b,c}$ feeding the ACC (see Fig. 10). Nevertheless some remaining voltage spikes are still found. That is why an additional capacitor C_0 and damping resistor R_0 in conjunction with a differential mode filter stage is installed (see Fig. 10, and [4]). The spectrum of the remaining voltage spikes is very wide due to the similarity to dirac pulses, while the amplitude of the spectral lines is small due to the limited energy. The series arrangement of inductors L_1, x-capacitors C_{x2}, capacitor C_0 and R_0 perform a series resonant tank (see Fig. 10). A suitable design is based on the idea, that the remaining voltage spikes should drop at L_1. Then formulas for C_0 and R_0 derive such as given in (6).

$$C_0 = \frac{6C_{x2}}{C_{x2}L_1\omega_s^2 - 1};\quad R_0 = \sqrt{\tfrac{1}{3}L_1(C_0^{-1} + (3C_{x2})^{-1})} \qquad (6)$$

C. Prototype

A prototype of the ACC was built, using two toroidal cores (*VAC vitroperm 500S 80*50*20* mm^3, $L_{1a} > 12$ mH, $L_{1b} > 48$ mH, $N_{1a} : N_{1b} : N_2 = 9 : 18 : 6$). For the half bridges (see Fig. 10) four *IRF840* are selected, driven by *IR2110* drivers. The pulse pattern for the half bridges are generated by a programmable Gate Array Logic (*GAL16V8*). For the capacitors C_{HB} of half-bridge A (B) operated with rectifiers switching frequency f_s ($3f_s$) a capacitance $C_{HB} = 300\,nF$ ($C_{HB} = 170\,nF$) was selected according to

(5). Damping resistors are added in series to the primary windings of the transformer.

Measurement Results

In Fig. 13 and Fig. 14 measurement results of the proposed ACC according to the schematic in Fig. 10 are depicted. In Fig. 13 again the original CM voltage measured at the input terminals of the rectifier as well as the recontructed CM voltage measured at the secondary windings of the transformer are shown. The high inductance of winding N_{1b} caused by the high turns number leads to low current levels.

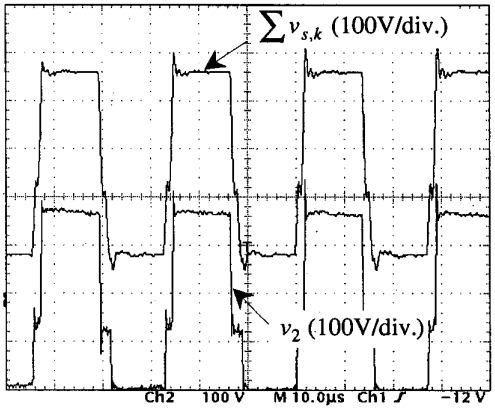

Fig. 13: CM-voltage v_0 at the rectifier input and rebuild voltage v_2 at secondary windings of the transformer (10µs / div.)

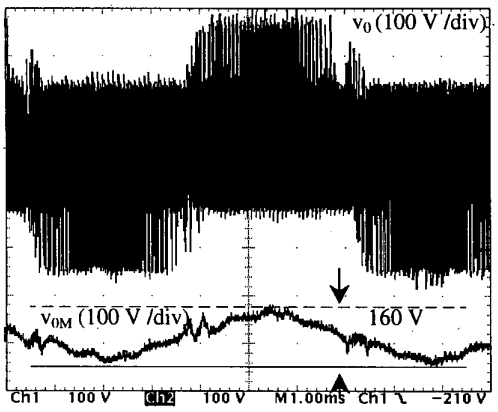

Fig. 14: Original CM voltage (upper trace) and CM voltage at mains terminals referred to center-tap (lower trace) at (1ms / div.)

IV. Summary and Conclusion

A new topology to compensate actively CM voltages in three-phase systems is presented. After a short discussion of methods presented to literature an analysis and modeling of CM voltages in Three-phase/Three-level systems is briefed. A new compensation scheme is presented, based on a five winding transformer with two separate primary windings and three secondary windings. Equations to model this transformer are given in conjunction with considerations for the design of the power circuitry. Simulation results verifying this concept are presented. Furthermore the design and verification of the concept is discussed based on elaborate measurement results. Measures to minimize or surpress the remaining voltage spikes resulting from non ideal compensation are given, too. Future work comprises an overall optimization of magnetics and the driving stage to reduce volume and costs aiming on high system efficiency at low extra costs. Finally this method should be integrated into an overall filter concept for Three-Phase systems, where stray inductances are considered.

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