QUASI-RESONANT-CONVERTERS FOR LOW OUTPUT VOLTAGE AND HIGH OUTPUT CURRENT

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Abstract

Recently introduced quasi-resonant-converter (QRC) create the supposition to raise switching frequency and power density of power supplies, by employing frequency- or pulse-width-modulated resonant-switches with reduced switching losses of the power devices. Examination of multiple resonant-switch-topologies with regard to the power switch stresses leads to the choice of a zero-current-switching- (ZCS) QRC for realisation of a converter with high output power, low output voltage and a wide range of load variation. The mathematical model of a buck-resonant-converter with parasitics of the power switches shows the influence of conduction losses to the voltage conversion ratio and efficiency. Theoretical results are verified by measurements. Since new IGBT devices seem to be suitable to reduce conduction losses of ZCS-resonant-switches, measurements were taken on a buck-converter with a variaty of IGBT power switches. Experimental results permit to calculate the total losses of the switching device and determine individual losses caused by different physical mechanism when the clock frequency is increased.

Keywords

Quasi–Resonant–Converters, High Power/Low Voltage, component Stress, Parasitic Effects, IGBT's

1. Introduction

Miniaturization of data processing units in computer systems goes along with the demand for volume and weight reduction of corresponding Power Supply Units. A usual way to raise the power density of SMPS is to increase the switching frequency. In order to reduce the switching losses with increased switching frequency the latest resonant switch concepts /1/.../4/ were introduced to manipulate the switch voltage or current. Even switching with zero voltage or current is possible.

The aim of this paper is to *determine a suitable resonant switch topology and technique* for an application in converters for *high current* and *low output voltage* with a large variation of load current. The substitution of equivalent quantities for inherent *parasitics* of the power switches into the model of a quasi resonant converter (QRC) with its selected resonant switch (RS) shows its *influence on the dc voltage ratio and efficiency.*

In the second part an investigation about an application of IGBT's in QRC's is briefed, which may be the basis of a comparative analysis concerning power losses of power MOSFET's and IGBT's in order to ascertain a cross–over switching frequency (f_{CO}), which would indicate an advantageous application of IGBT's.

Part 1

2. Resonant switches

2.1 Zero–current–switched resonant switch (ZCS–RS)

For a turn–on controlled or better known as *zero–current resonant switch* /1/ the transistor is located in a parallel resonant circuit. The transistor is positioned in series with the resonant inductance, in order to switch on and off with zero current; hence the current slope is limited, see fig. 1a.

The transistor *switch–on can be controlled*, while the *switch–off* occurs *constrained with zero–current.* Thus, the *switch–on time* of the active switch is nearly *constant. Condition* for *zero–current switching* is that the amplitude of the tank capacitance current ($\hat{i}_C$) is greater than the resonant switch current i_{RS}, which is nearly constant in the active state of the resonant switch. In this mode of operation with zero–current switching the resonant switch is able to switch in a range of $0 \leq \hat{i}_{RS} \leq \hat{i}_C$, whereby $\hat{i}_C$ follows when the voltage on C at turn on of switch S and tank impedance $Z_0 = \sqrt{L/C}$ are known. A disadvantage of this topology is the *non lossless turn–on* caused by the output capacitance of the transistor and the high current stress of the transistor for all load states with $\hat{i}_L = \hat{i}_C + i_{RS}$ and $\hat{i}_L \geq 2\,\hat{i}_{RS\,max}$ for maximum load current.

2.2 Zero–voltage–switched Resonant switch (ZVS–RS)

For the *turn–off controlled* or *zero–voltage resonant switch* /2/ the transistor is located in a series resonant circuit. The transistor is positioned parallel to the tank capacitance; hence the switch–on and off works with zero–voltage switching and the voltage slew rate is limited, see fig. 1b.

Switching–off is controlled, while *switching–on occurs constrained* with a zero voltage crossing of u_C. Thus the *off–state time* of the active switch is nearly *constant. Condition* for *zero–voltage switching* is that the amplitude of the tank inductance $\hat{u}_L$ is greater than the off-state switch voltage u_{RS}, with u_{RS} being constant in the passive state of the resonant switch. Hence, this operational mode with zero–voltage switching of the ZVS–RS is given, if $\hat{u}_L > u_{RS}$, with $\hat{u}_L$ given by the current of the tank inductance at turn–off of S and the tank impedance $Z_0 = \sqrt{L/C}$.

Disadvantageous with zero–voltage switching is the fact, that current i_{RS} shouldn't be lower than u_{RS}/Z_0. Note that the voltage stress for the transistor is already $\hat{u}_C \geq 2u_{RS}$. An increase of the resonant switch current to $10 \cdot u_{RS}/Z_0$ is accompanied by a voltage stress of $\hat{u}_C > 11 \cdot u_{RS}$.

The neccessary *frequency modulation* is a common fact for both resonant switch types, which follows from the constant on– resp. off–time of the active switch.

2.3 Pulse–Width Modulated Resonant switches (PWM–RS)

Adding an *auxiliary switch* S_{aux} into the resonant circuits /4/ results in resonant switches, which may be controlled by pulse–width modulation, see fig. 1c,d. Task of this auxiliary switch is to *delay the resonant process* after the switch–on (switch–off) of the main switch in case of the ZCS–RS (ZVS–RS) in order to vary the switch–on (switch–off) time with constant switching frequency.

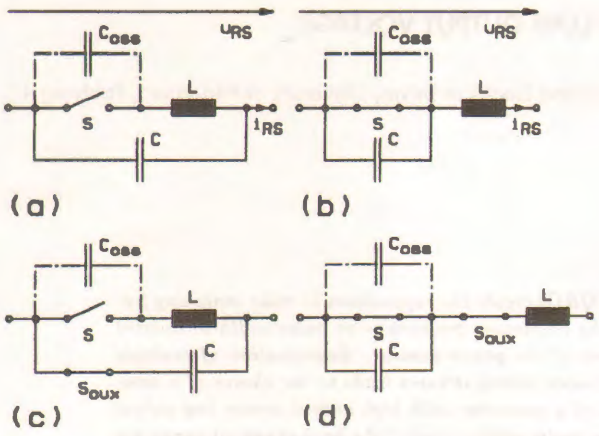


Fig. 1: Resonant switch topologies
(a) with zero-current switching (ZCS-RS)
(b) with zero-voltage switching (ZVS-RS)
(c) Pulse-width modulated with zero-current switching (ZCS-PWM-RS)
(d) Pulse-width modulated with zero-voltage switching (ZVS-PWM-RS)

Advantages of the PWM-RS are to utilize the well known principles of control based on pulse width modulation and to design filter elements for *constant switching frequency*. On the other hand the component count and power losses due to the additional auxiliary switch is increased and the desired zero-voltage switching cannot be realized in actual fact by the PWM-ZVS-RS.

2.4 Quasi-Square Resonant Switches (QSS)

The recently introduced resonant switches with quasi-square waveforms /5/ were investigated in /6/ with respect to their qualification for high current applications and low output voltage, but should be quoted here only because lack of space.
A supplement paper to the one by Vorperian /7/ will be presented soon.

3. Quasi-Resonant-Converters (QRC)

The mentioned resonant switches of chapter 2 are suited in principle to *substitute the active switch* for all common pulse-width modulated converter topologies known in order to reduce certain types of dynamic losses.
For the intended application in high current power supplies the basic buck-type is the foundation for nearly all converter topologies. Hence the following is reduced simply on the buck-topology.
Converters with resonant switches working in that mode described in chapter 2 are termed quasi-resonant converters. This terminology is derived from the fact that the task of the resonant circuit is simply to give the waveform of switch current (switch voltage) a sinusoidal shape, whereby zero-current switching (zero-voltage switching) is achieved. Analogous to the conventional switching technique energy transfer occurs non-continuously. Due to the fact that the initial values of the tank quantities are constant and well known (except for quasi-square converters) the analysis is far easier than for resonant converters, see e.g. expressions for the voltage conversion ratio in /6/.

3.1 Typical waveforms for QRC's

Fig.2 gives two alternatives for frequency modulated quasi-resonant buck-converters: fig. 2a with ZCS-QRS and fig. 2b with ZVS-QRS. A common fact for both topologies is the bi-directional sinusoidal waveform – hence this mode is defined as "fullwave mode" (FWM). According to the arrangement of diodes in combination with the transistor a unidirectional energy flow corresponds with the "halfwave mode" (HWM). Quasi resonant converters working in FWM behave like a constant voltage source with narrow band frequency modulation

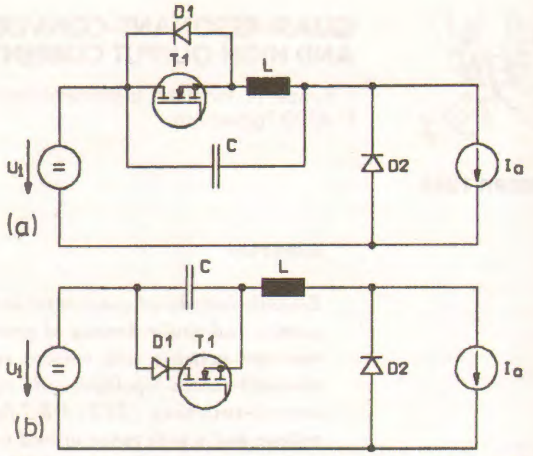


Fig. 2: Quasi-resonant buck-converter for FWM and ideal filter/load network
(a) with zero-current switching
(b) with zero-voltage switching

to control wide load variations. Optimization of output filter components may be performed easily.
In fig. 3 waveforms of the tank quantities for FWM are shown whereby the duality of both topologies can be concluded.

3.2 Stress comparison of resonant switches

Estimating the stress of the switches in QRC's (see fig.2) one has to distinguish between quantities, which can be dealt mathematically for an ideal converter model and those additional electrical stresses produced by parasitic effects of the real switches.

3.2.1 Component stress for the ideal model

a) ZCS-QRC

The *maximum voltage stress* of the transistor for the ideal model of the ZCS-QRC is fixed to the input voltage U_i independent of the actual load current. The maximum on-state current of the transistor is load depending in a range of $I_a max < U_i/Z_0 < i_{T1} \leq U_i/Z_0 + I_a max$. As already mentioned it results to $i_{T1} max > 2I_a max$ for zero-current switching. Thus a *higher current stress* in terms of RMS-values derives compared to conventional buck-converters and hard switching.

b) ZVS-QRC

For the ideal model of the ZVS-QRC the switch current is limited to the actual value of the load current; hence, it follows $i_s \leq I_a$ and $i_s max = I_a max$. This advantage is drastically reduced because of the high and load depending *voltage stress* of the transistor, see chapter 2.2.
The sensitive increase of voltage stress for the transistor with a variation of load current causes high on-state losses for full load because the on-state resistance e.g. for a power MOSFET increases rapidly with the maximum voltage required. Consequently the zero-voltage switching technique doesn't suit for a buck-converter if large load variations are required.

3.2.2 Additional stresses by parasitic effects

a) ZCS-QRC

The inherent disadvantage of this switching technique is that switching on the transistor causes discharge of the output capacitance of the switch consisting of T_1 and D_1 leading to additional power losses $P_{VC} = 1/2 \cdot (C_{OSS} + C_D) \cdot U_i^2 \cdot f_s$. In addition the turn-off characteristic of diode D_1 causes an induced voltage by the tank inductance in addition to the input voltage U_i. The stored energy of tank inductance L generates a high frequent ringing due to L and C_{OSS} and C_D, causing additional losses.
The switching conditions for the freewheeling diode of the ZCS buck converter are well behaved, because of the fixed blocking voltage by the tank capacitance, if parasitic lead inductances in the respective mesh U_i (resp. C_i) - C - D_2 can be avoided.

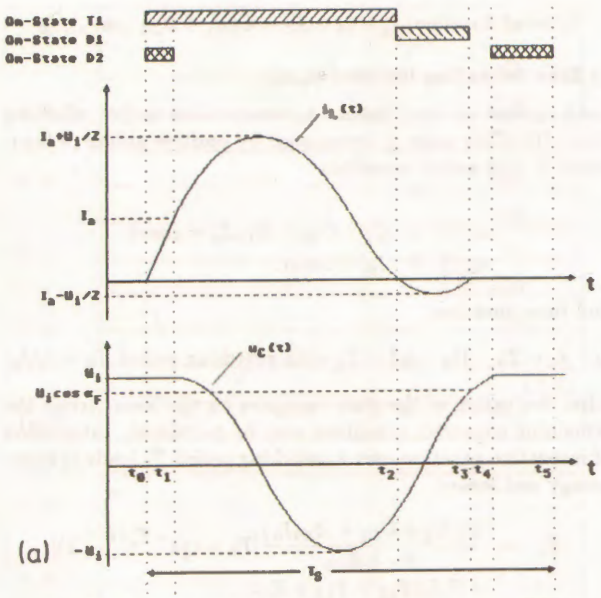


Fig. 3: Waveforms for a QR buck-converter for FWM
(a) with zero-current (b) with zero-voltage switching

b) ZVS-QRC

The ZVS-buck-converter qualifies also for highest switching frequencies because lossy discharge of the output capacitance of the transistor doesn't take place. The voltage stress of the freewheeling diode caused by it's turn-off characteristic is a problem.

3.2.3 Selection criteria according to component stress

There is a great variety of topological very similar circuits in each group of switching technique, which differ only by the location of the tank elements L and C called M, L_1, L_2-types, see /3/. But variations of e.g. ZCS-buck-QRC's show identical characteristics in terms of dc models and the already mentioned power switch stress. They differ in respect to the stress of tank elements, input voltage and requirements concerning the output filter. Further investigations led to the topology in fig. 4 of the ZCS-QR-buck-converter for the application under study.

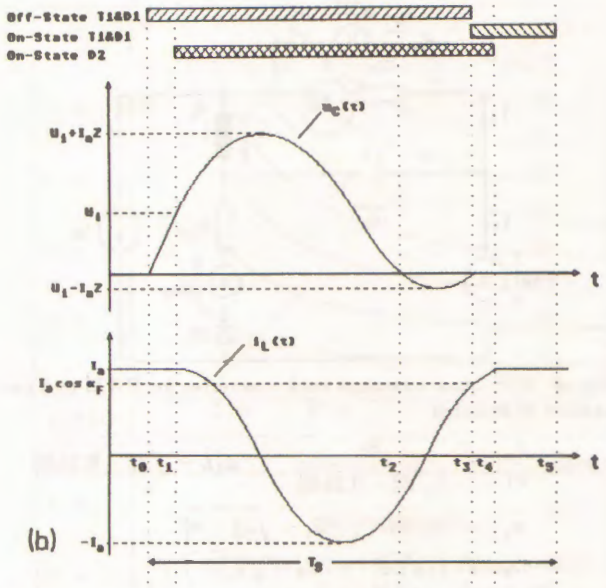
3.3 Model of the ZCS-QR-buck-converter with parasitics

For the ideal model of a quasi-resonant buck-converter with ZCS-RS, driven in half-wave-mode (with unidirectional switch) and full-wave-mode (with bidirectional switch), derivations with respect to the voltage conversion ratio and efficiency are given in literature /1/.../3/. In these publications deviations, which occur when theoretical results for the ideal model are compared to measured results of a breadboard converter, are attributed to the power device losses. Until now quantitative calculations to investigate these facts of case have not been published yet.

Because in ZCS-QRC conduction losses of the semiconductor power switches are dominant, the mathematical model of a buck-converter (see fig. 4) is extended to include parasitic equivalent elements of the power devices, represented by voltage sources and series resistances, assuming that the on-state losses of switches represent the dominant share of total losses. The L_fC_f-low-pass filter with load R can be comprehended as a current sink I_a to reduce system order. This assumption is admissible, if the ripple current of the filter inductance is low. Notice that dynamics of the power converter is not of interest here but a modification of the dc model.

State space description of the second order system results in solutions for the state variables $u_C(t)$ and $i_L(t)$, various switch currents and the input current.

There are four switching stages per switching cycle analogue to the analysis of the ideal model:



a) Linear Interval $[t_0, t_1]$
b) Resonant Interval (T conducts) $[t_1, t_2]$
c) Resonant Interval (D1 conducts) $[t_2, t_3]$
d) Capacitor discharging Interval $[t_3, t_4]$
e) Free wheeling Interval $[t_4, t_5]$

The analysis is briefed for one switching cycle T_S in terms of state quantities as follows:

a) Linear Interval $[t_0, t_1]$

The transistor current rises with limited slew rate by positive gating the active switch T while the free wheeling current falls with the same rate. For this analysis the voltage variation of the tank capacitance due to the variation of current passing D2 is neglected, because the error between approximated and exact solutions is negligible.

It follows with initial conditions:

$i_L(t_0) = -I_a \quad ; \quad u_C(t_0) = U_i + u_{D2}$ (Approx.)

$$i_L(t) = -I_a e^{-(t\ -t_0)/\tau} + \frac{U_i + U_{D2} - R_T I_a}{R_T + R_{D2}} \left(1 - e^{-(t\ -t_0)/\tau}\right)$$

with $\tau = L/(R_T + R_{D2})$

This time interval continues until the load current has commutated to transistor T. Then the tank current becomes $i_L(t_1) = 0$ with time interval:

$$t_1 - t_0 = T_a = -\tau \cdot \ln \frac{U_i + U_{D2} - R_T I_a}{U_i + U_{D2} + R_{D2} I_a}$$

b) Resonant interval (on-state of T) $[t_1, t_2]$

After blocking of the free wheeling diode D2 the load is directly sourced; meanwhile the resonant circuit rings.

Hence, we get with initial values of the state variables

$$u_C(t_1) = U_i + U_{D2} \quad ; \quad i_L(t_1) = 0 \qquad \text{and}$$

$$\begin{bmatrix} \dot{u}_C \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} 0 & -1/C \\ 1/L & -R_T/L \end{bmatrix} \begin{bmatrix} u_C \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ R_T \end{bmatrix} I_a$$

the solutions of the second order system:

$$u_C(t) = \left(U_i + U_{D2} - I_a R_T\right) e^{-\sigma_1 (t - t_1)} \left[\cos\omega_1(t - t_1) + \frac{\sigma_1}{\omega_1} \sin\omega_1(t - t_1)\right] + R_T I_a$$

$$i_L(t) = \frac{U_i + U_{D2} - R_T I_a}{\omega_1 L} e^{-\sigma_1 (t - t_1)} \sin\omega_1(t - t_1)$$

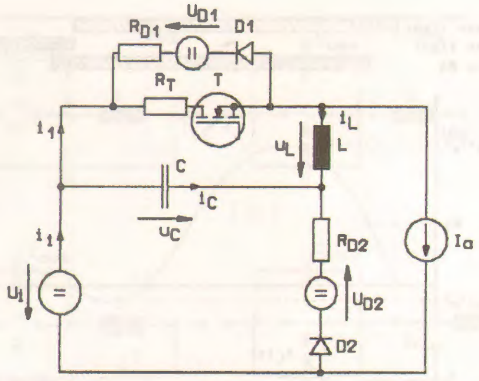


Fig. 4: ZCS–quasi–resonant buck–converter for FWM and parasitics of switches

$$\text{with} \quad \frac{\sigma_1}{\omega_1} = \frac{R_T}{2\sqrt{Z_0^2 - 0.25R_T^2}} \quad , \quad \omega_1 L = \sqrt{Z_0^2 - 0.25R_T^2}$$

$$\sigma_1 = R_T/2L \quad , \quad \omega_1 = \sqrt{\omega_0^2 - \sigma_1^2}$$

$$\omega_0 = 1/\sqrt{LC} \quad , \quad Z_0 = \sqrt{L/C}$$

During the first zero crossing of the switch current $i_1(t) = i_L(t) + I_a$ the current changes from transistor T to its antiparallel diode D1 after the interval duration $t_2 - t_1 = T_{b1}$, which calculates with equation:

$$i_1(t_2) = \frac{U_i + U_{D2} - R_T I_a}{\omega_1 L} e^{\sigma_1(t_2 - t_1)} \sin\omega_1(t_2 - t_1) + I_a \stackrel{!}{=} 0$$

This transcendental equation has to be solved for T_{b1} after the converter has been designed.

c) Resonant stage (on–state of D1) $[t_2, t_3]$

After the current has diverted from the active switch to D1 it follows with initial conditions for the state variables

$$u_C(t_2) = u_{C2} \quad ; \quad i_L(t_2) = -I_a \qquad \text{and}$$

$$\begin{bmatrix} \dot{u}_C \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} 0 & -1/C \\ 1/L & -R_{D1}/L \end{bmatrix} \begin{bmatrix} u_C \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ 1/L \end{bmatrix} (U_{D1} - R_{D1} I_a)$$

the solutions of the second order system:

$$u_C(t) = (u_{C2} + U_{D1} - R_{D1} I_a) e^{-\sigma_2(t - t_2)} \left[\cos\omega_2(t - t_2) + \frac{\sigma_2}{\omega_2} \sin\omega_2(t - t_2)\right] + \frac{I_a Z_0^2}{\omega_2 L} e^{-\sigma_2(t - t_2)} \sin\omega_2(t - t_2) - (U_{D1} - R_{D1} I_a)$$

$$i_L(t) = \frac{u_{C2} + U_{D1} - 0.5 R_{D1} I_a}{\omega_2 L} e^{-\sigma_2(t - t_2)} \sin\omega_2(t - t_2) - I_a e^{-\sigma_2(t - t_2)} \cos\omega_2(t - t_2)$$

with coefficents analogue to time interval $[t_1, t_2]$

With the second zero crossing of switch current $i_1(t) = i_L(t) + I_a$ the antiparallel diode D1 blocks and the constant load current is lead by the series circuit of L and C.

Equation for time interval $t_3 - t_2 = T_{b2}$:

$$i_1(t_3) = \frac{u_{C2} + U_{D1} - 0.5 R_{D1} I_a}{\omega_2 L} e^{-\sigma_2(t_3 - t_2)} \sin\omega_2(t_3 - t_2) - I_a e^{-\sigma_2(t_3 - t_2)} \cos\omega_2(t_3 - t_2) \stackrel{!}{=} 0$$

d) Capacitor discharging interval $[t_3, t_4]$

For the interval with constant dischargement of tank capacitance C with load current I_a we obtain with initial conditions:

$$i_L(t_3) = I_a \quad ; \quad u_C(t_3) = u_{C3}$$

$$u_C(t) = \frac{I_a}{C}(t - t_3) + u_{C3}$$

This time interval lasts until the tank capacitance voltage $u_C(t)$ becomes $u_C(t_4) = U_i + U_{D2}$ and D2 starts conducting.

Interval duration: $t_4 - t_3 = T_c = C(U_i + U_{D2} - u_{C3})/I_a$

e) Free–wheeling interval $[t_4, t_5]$

Load current at time instant t_4 commutates to free wheeling diode D2. This stage is terminated by positive gating of transistor T. The actual equations

$$u_C(t) = U_i + U_{D2} + R_{D2} I_a = const.$$
$$i_L(t) = I_a = konst.$$

and time duration:

$t_5 - t_4 = T_s - (t_4 - t_0) = T_d$ with switching period $T_s = 1/f_s$.

After derivation of the state variables for the lossy circuit the remaining converter quantities may be calculated. Integration of respective equation over a switching period T_s leads to input energy and losses:

$$E_i = \frac{U_i(U_i + U_{D2} + R_{D2} I_a)}{R_T + R_{D2}} [T_a + \tau(e^{-T_a/\tau} - 1)] + U_i I_a (T_{b1} + T_{b2} + T_c)$$

The output energy calculates to $E_a = I_a U_a T_s$.

The power losses consist of four portions, assuming that no losses are generated during discharging state. The indices refer to the termed intervals.

$$E_v = E_{va} + E_{vb1} + E_{vb2} + E_{vd}$$

with E_{va}: losses during commutating interval of D2 to T
E_{vb1}: losses during resonant interval (on–state of T)
E_{vb2}: losses during resonant interval (on–state of D1)
E_{vd}: losses during free wheeling interval

$$E_{va} = (R_T + R_{D2}) \left\{ \frac{\tau}{2}(a + b)^2 \left(1 - e^{-2T_a/\tau}\right) - 2\tau(b^2 + ab) \left(1 - e^{-T_a/\tau}\right) + b^2 T_a \right\} + (2R_T I_a - U_{D2}) \left\{ \tau(a + b) \left(e^{-T_a/\tau} - 1\right) + bT_a \right\} + R_T I_a^2 T_a$$

$$E_{vb1} = R_T I_a^2 T_{b1} + R_T \left\{ c^2 \frac{\omega_1^2}{4\omega_0^2} \left[\frac{1}{\sigma_1} \left(1 - e^{-2\sigma_1 T_{b1}}\right) - \frac{2}{\omega_1} e^{-2\sigma_1 T_{b1}} \sin\omega_1 T_{b1} \left(\frac{\sigma_1}{\omega_1} \sin\omega_1 T_{b1} + \cos\omega_1 T_{b1} \right) \right] \right\} + R_T I_a \left\{ c \frac{\omega_1}{\omega_0^2} \left[1 - e^{\sigma_1 T_{b1}} \left(\cos\omega_1 T_{b1} + \frac{\sigma_1}{\omega_1} \sin\omega_1 T_{b1} \right) \right] \right\}$$

$$E_{vb2} = R_{D1} \left\{ d^2 \left[\frac{\omega_2^2}{4\omega^2} \left(\frac{1}{\sigma_2} \left(1 - e^{-2\sigma_2 T_{b2}}\right) - \frac{2}{\omega_2} e^{-2\sigma_2 T_{b2}} \sin\omega_2 T_{b2} \left(\frac{\sigma_2}{\omega_2} \sin\omega_2 T_{b2} + \cos\omega_2 T_{b2} \right) \right) \right] + ad \left[\frac{\omega_2}{2\omega_0^2} \left(e^{2\sigma_2 T_{b2}} \left(\cos 2\omega_2 T_{b2} + \frac{\sigma_2}{\omega_2} \sin 2\omega_2 T_{b2} \right) - 1 \right) \right] + a^2 \left[\frac{\omega_2^2}{4\omega_0^2} \left(\frac{1}{\sigma_2} \left(1 - e^{\sigma_2 T_{b2}}\right) + \frac{2\sigma_2}{\omega_2^2} - \frac{2}{\omega_2} e^{-\sigma_2 T_{b2}} \cos\omega_2 T_{b2} \left(\frac{\sigma_2}{\omega_2} \cos\omega_2 T_{b2} - \sin\omega_2 T_{b2} \right) \right) \right] \right\} + (R_{D1} I_a - U_{D1} I_a) T_{b2} + (2R_{D1} I_a - U_{D1}) \left\{ \frac{\omega_2}{\omega_0^2} \left[d \left(e^{-\sigma_2 T_{b2}} \left(\cos\omega_2 T_{b2} + \frac{\sigma_2}{\omega_2} \sin\omega_2 T_{b2} \right) - 1 \right) + a \left(e^{\sigma_2 T_{b2}} \left(\sin\omega_2 T_{b2} - \frac{\sigma_2}{\omega_2} \cos\omega_2 T_{b2} \right) + \frac{\sigma_2}{\omega_2} \right) \right] \right\}$$

$$E_{vd} = \left(R_{D2} I_a^2 + U_{D2} I_a\right) T_d$$

with the following substitutions

$$a = I_a \quad ; \quad b = \frac{U_i + U_{D2} - R_{D2} I_a}{R_T + R_{D2}}$$

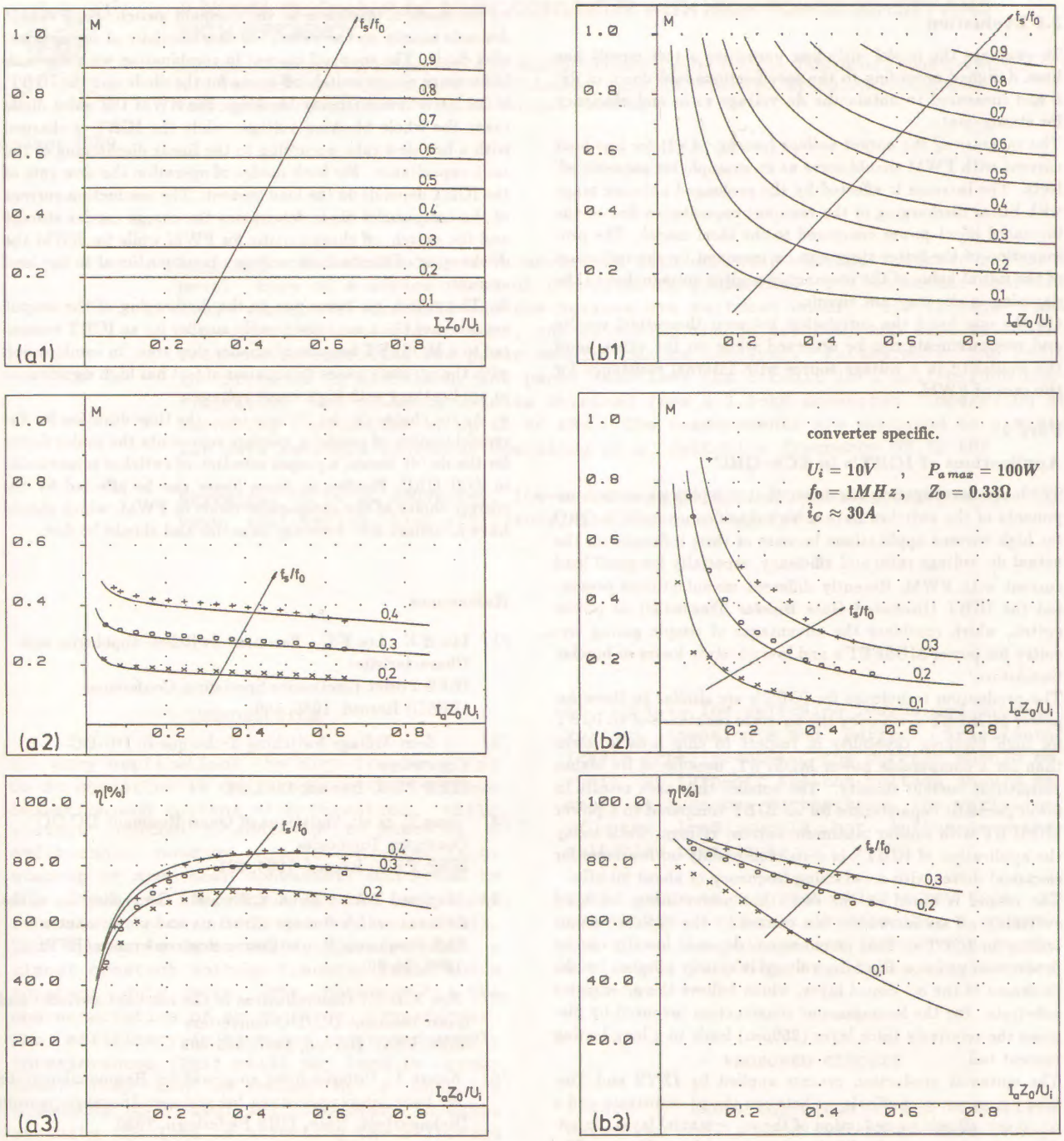


Fig. 5: DC-voltage ratio M and efficiency η versus normalized output current for a ZCS-QR buck-converter.

(a1) for FWM and ideal conditions, (b1) dito for HWM,
(a2) for FWM incl. parasitics, (b2) dito for HWM,
(a3) for FWM incl. parasitics (b3) dito for HWM

— computed results for model with parasitics
+, o, x measurement results for the breadboard converter

$$c = \frac{U_i + U_{D2}}{\sqrt{Z_0^2 - 0.25R_T^2}} \frac{R_T I_a}{}, \quad d = \frac{U_{Cb1} + U_{D1}}{\sqrt{Z_0^2 - 0,25R_{b2}^2}} \frac{0,5R_{D1} I_a}{}$$

3.4 DC conversion ratio and efficiency

Formulating the energy balance we are in a position to calculate the modified dc voltage ratio and efficiency. Hence, plots of the dc ratio and efficiency are obtained in terms of the normalized load current and switching frequency. Since the presentation of the dc-voltage ratio for the ideal model corresponds to the one of the model including parasitics direct comparison can be made (see fig. 5).

a) DC-voltage ratio M

For steady-state of the converter an operating point of the dc-voltage ratio versus normalized switching frequency is determined by U_i, I_a and f_s resp. $M = U_a/U_i$, I_aZ_0/U_i and f_s/f_0 in normalized form.
The modified dc-voltage ratio results as

$$M = \frac{U_a}{U_i} = \frac{E_i}{I_a U_i T_S} \frac{E_v}{} = \frac{P_i}{I_a U_i} \frac{P_v}{}$$

with input power P_i and power losses of switches P_v.

b) Efficiency η

Analogous we find $\eta = \frac{E_i}{E_i} \frac{E_v}{} = \frac{P_i}{P_i} \frac{P_v}{}$

3.5 Evaluation

To evaluate the model including parasitics a test circuit has been designed according to the specifications laid down in fig. 5 and measured to obtain the dc–voltage ratio and efficiency for steady–state.

The *increase of the output voltage* (see fig. 4.a2) for low load current with FWM should serve as an example for parasitic effects. The increase is affected by the prolonged network stage with linear discharging of the resonant capacitance due to the increased input power compared to the ideal model. The prolongation of the latter stage can be reasoned by the reduction of the initial value of the resonant capacitor voltage due to the damping in the resonant circuit.

On the one hand the correlation between theoretical results and measurements can be observed while on the other hand the similarity to a voltage source with internal resistance for the case of FWM.

Part 2

Applications of IGBT's in ZCS–QRC

The latter investigation has shown that damping parasitic components of the switches have a high significance in ZCS–QRC for high current applications because of their influence on the actual dc–voltage ratio and efficiency, especially for small load current with FWM. Recently different manufacturers presented the IGBT (Insulated Gate Bipolar Transistor) as power switch, which combines the advantages of simple gating circuitry for power MOSFET's and low on–state losses of bipolar transistors.

The production techniques for IGBT's are similar to those for power MOSFET's, whereby the on–state resistance of an IGBT for high blocking capability in respect to chip area is lower than for a comparable power MOSFET, because of its higher permissible current density. The smaller chip area results in lower parasitic capacitances for an IGBT compared to a power MOSFET with similar maximum current ratings. Until today the application of IGBT's is restricted mainly on inverters for electrical drives with a switching frequency of about 20 kHz.

The reason is based on the fact, that power losses for hard switching–off are increasing fast caused by the typical current tailing for IGBT's. This phenomenon depends heavily on the production process. Blocking voltage is mainly affected by the thickness of the n^- doped layer, which follows the p^+–emitter substrate. For the homogeneous construction favoured by Siemens the relatively thick layer ($250\mu m$) leads to a long lasting current tail.

The epitaxial production process applied by IXYS and Toshiba carries an n^+ buffer layer between the p^+–substrate and a n^-–layer, allowing a reduction of the n^- epitaxial layer. In addition the charge carrier lifetime is reduced by radiation. The resulting IGBT type offers a short current tail, which on its side depends on the previous on–state current /9/.

The idea of applying the IGBT in ZCS–QRC is obvious because an off-state time – before a blocking voltage is applied – is guaranteed by this switching technique. To clarify this matter of fact measurements with IGBT's of various manufacturers were conducted at a test circuit with an input voltage of 200 V. They lead to the following conclusions about the suitability of IGBT's for this switching technique and converter topology:

1. To utilize the advantage of lower on–state losses of IGBT's its switch–on time has to be long enough in order to switch–on effectively the bipolar transistor. This requirement limits the maximum useful switching frequency.

2. The so called du/dt losses represent the highest portion of the switch–off losses of IGBT's. These losses go along with a short current peak, which is based on the non fully recombined charge carriers and a high slew rate of blocking voltage. This effect can be moderated by a sufficient off-time for the transistor, implying a limitation of the switching frequency. On the other hand the slew rate of the recurrent blocking voltage is affected by the mode of operation on the resonant switch. For FWM it depends mainly on the switch–off characteristic of the antiparallel diode. The snap–off current in combination with the tank inductance causes switch–off losses for the diode and the IGBT, if the latter is not already blocking. For HWM the series diode takes the whole blocking voltage, while the IGBT is charged with a low slew rate, according to the linear discharging of the tank capacitance. For both modes of operation the slew rate of the IGBT depends on the load current. The conduction current of the antiparallel diode determines the charge carrier storage and the switch–off characteristic for FWM while for HWM the discharging of the tank capacitance is proportional to the load current.

3. The switch–on losses due to the discharging of the output capacitance C_{OSS} are considerably smaller for an IGBT compared to a MOSFET because of smaller chip area. In combination with the on–state losses this matter of fact has high significance in applications with high input voltages.

4. As the charge carrier lifetime resp. the time duration for the recombination of minority carriers represents the major factor for the du/dt–losses, a proper selection of switches is inevitable in ZCS–QRC. Further on these losses can be affected by the correct choice of the antiparallel diode in FWM, which should have a distinct soft–recovery behavior and should be fast.

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