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COMPARATIVE ANALYSIS OF HIGH CURRENT COMPONENTS IN PWM CONTROLLED CONVERTER TOPOLOGIES QUALIFIED FOR HIGH OUTPUT POWER AND LOW OUTPUT VOLTAGE

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Abstract

A comparative analysis of six square wave converter topologies (SMPS), selected for high output power and low output voltage, is performed for the secondary- side components. This analysis is realized for chokes, the capacitive components and secondary- side power rectifiers under consideration of parasitics. Objective is with regard to progressive miniaturization of SMPS's, to increase the power density and to reduce power losses by choice of a suitable circuit concept. The obtained results are normalized in terms of converter specifications and operational parameters. Hence general conclusions are gained. A comparative design example is worked out for a 5 V/100 A converter.

Keywords

Switch Mode Power Supplies, High Power/ Low Voltage, Topologies Comparison, Power Density Increase

Introduction

Progress in the field of VLSI-technology is to increase data processing power accompanied by a reduction of size of data processing circuits although their complexity is increasing. On one hand miniaturization of faster data processing units is opposed by their high power consumption, but on the other hand it goes along with the demand for power supply units with high power density. So far computers of any type are supplied nearly totally by power converters with hard commutations (SMPS) and the major supply burden with ever increasing importance and share of the total power is carried by the low voltage converter for $3.3 \div 5\ V$ with some hundred watt up to some megawatt.

Therefore it is surprising, that until today there is no established comparative analysis about the suitability of power converter topologies for this specific but most important range of application, as the contradicting statements indicate in various papers /1//2//3//4/ about favourable topologies for specific power ranges and the differing topologies in manufactured high power supplies /5/.

Consequently the question arises:

Are there topologies in favour of others with regard to component stress and power density or is the selection of power converter topologies an arbitrary matter compared to other power density increasing/influencing measures like the alteration of the supply system, switching frequency, filter method and cooling type or a suitable shape of the power supply package together with an application of specific materials, components and modern building techniques?

Many of those criteria mentioned above are predetermined by the applicant specifications but this isn't true for the field of topology. But because of the broad and lengthy character of the comparative analysis of topologies it cannot be reported here completely. Having preselected suitable topologies and calculated electrical stresses for components of the power circuits the analysis of high current components is focussed instead.

After determining the design parameters, the so far neglected parasitics are taken into consideration for the approximative comparative analysis concerning efficiency and size of the high current components without alteration of prederived stress-describing functions. This pragmatical way was applied, because the direct inclusion of parasitics would cause a vast and to our extend unneccessary increase of algebra compared with the improvement achieved.

Selection of suitable topologies

Suitable solutions for efficiently working high power and low output voltage power converters are Switch Mode Power Supplies with a power flow, as continuous as possible, i.e. the group of forward converters. They allow to minimize the stored energy - thus the volume per power - and the electrical stress on power switches. In this paper we refer to the classical (non - resonant) switch mode power conversion, processing with nearly square or rectangular voltage and current waveforms.

A distinction of the selected topologies is due to:

- **single ended** converters
  (forward-, two-transistor-forward- and Ćuk-converter)
- **double ended** converters
  (half-, full bridge and push pull-converter)

The latter are clocked twice per switching period T_S, while the former are clocked once.

The preselected converter topologies are represented in **table 1.** The ideal DC - conversion ratios are assumed to be known where

$U_{a,i}$: Average Value of output -, input voltage
D : duty cycle
$\ddot{u}_1$: ratio of transformation

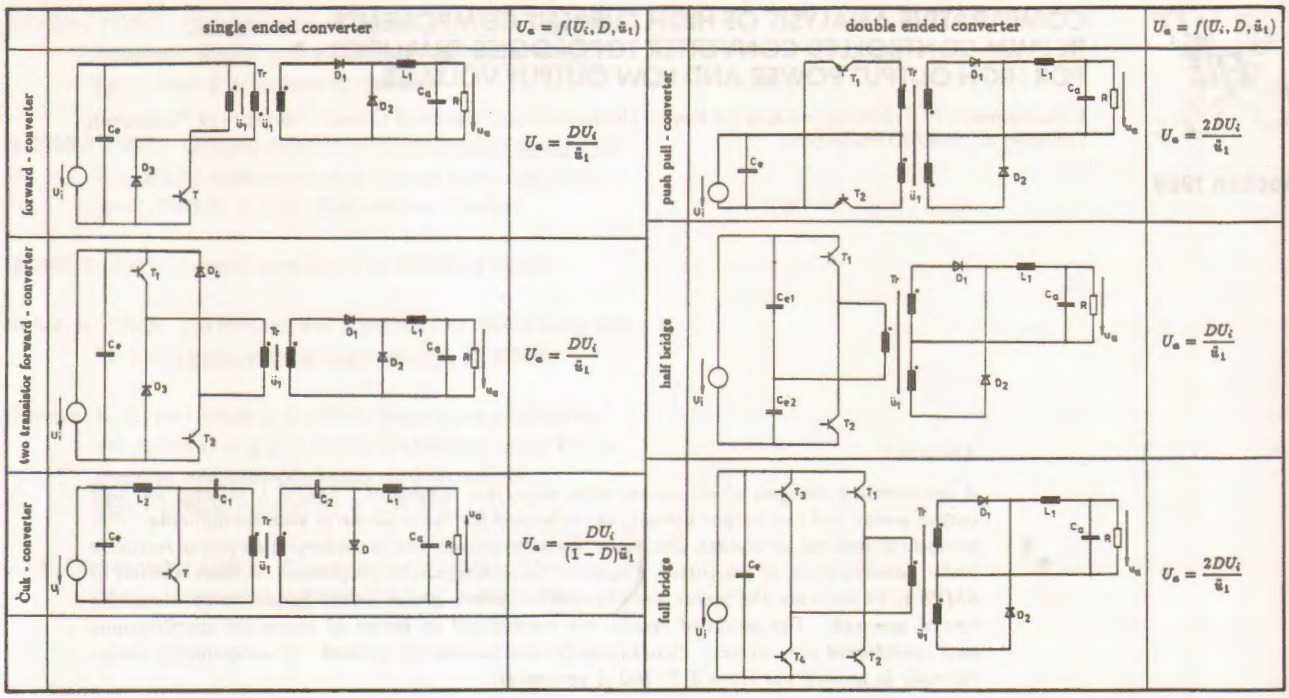

table 1: selected converter topologies

Stresses of components of the power circuit

The maximum rating of the components of the power circuit is due to limits which must not be exceeded in periodical operation or at step loads. They determine type, costs, reliability, total size of components, cooling facilities and efficiency.
The relevant stress quantities are X_{AV} ,X_{RMS} and x_{max} values of currents and/or voltages.

Location of stresses

In order to conduct a comparative analysis the relevant stress quantities have to be derived for the respective converters. They are obtained by solving a set of equations for each converter and their constraints for steady state.
If the following assumptions and approximations are taken results can be obtained, which may be interpreted easily and can be derived with reasonable efforts:

- Input and output voltages are assumed to be constant, because of the insignificant ripple.
  Thus, the buffer and filter capacitors C_a and C_e don't occur in the results. The currents $i_{ce}(t)$ and $i_{ca}(t)$ are calculated in that way in order to obtain $i_i(t)$ and $i(t)$ as DC - currents. Hence, the capacitive currents equal the AC portions of $i_i(t)$ and $i(t)$ respectively. Obviously the system order is reduced considerably for the comparative analysis.
- For the transformer an ideal coupling between the primary and secondary windings is assumed, whereby hard commutations may take place.
  Initially copper - and core losses are neglected, but the magnetizing current is considered.
- The converters are assumed to work in the contineous conduction mode (contineous filter current $i_a(t)$) only.
- The other components are first taken to be ideal.
- Single ended converters with magnetic flux reset means are considered to be demagnetized before the transistor switches on again.
- All capacitors currents and voltages on the magnetic components don't show DC - values for steady state.
- The equations for the Ćuk converter description contain cosine and sinewave functions, which are linearized because resonant frequencies of the resulting waveforms are much smaller than the switching frequency.

For the selected example - the two-transistor-forward converter (see **figure 1**) - the resulting waveforms for the power components (under mentioned conditions) are shown in **figure 2**. Obviously the calculations of the respective X_{AV} ,X_{RMS} and x_{max} figures follow only for relevant stress - quantities (see **table 2**). Because of the lack of space, only those quantities are listed in table 2, which are meaningfull for the analysis of the secondary sided network.

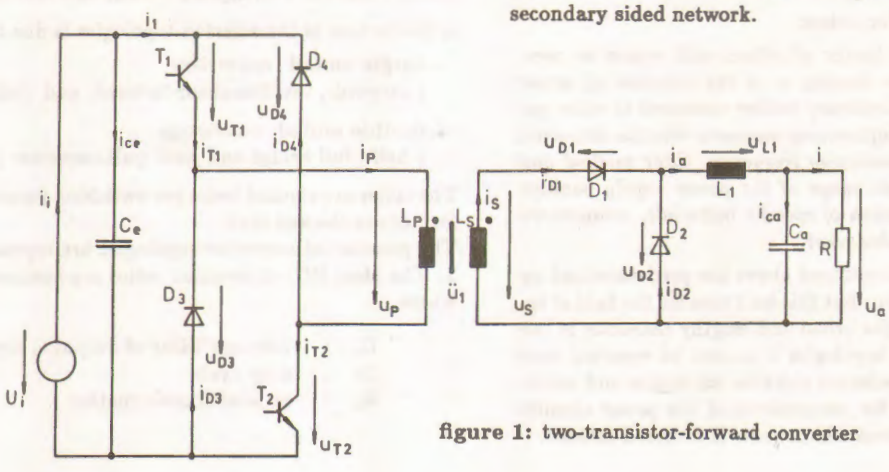

figure 1: two-transistor-forward converter

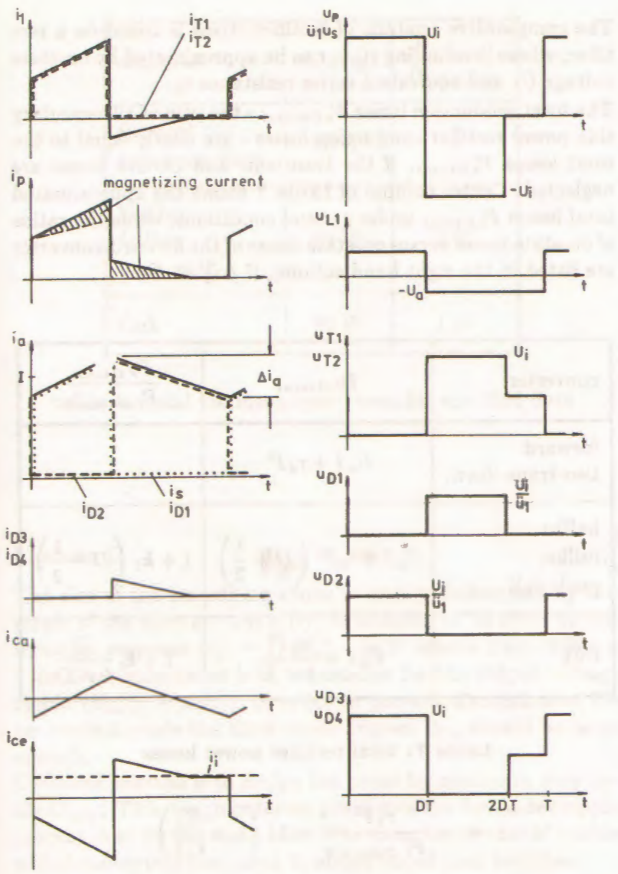

figure 2: waveforms for the two-transistor-forward converter

component		X_{AV}	X_{RMS}	x_{max}
L_1	$i_a(t)$	I	$\sqrt{I^2+\frac{\Delta i_a^2}{12}}$	$I+\frac{\Delta i_a}{2}$
Transf.	$i_S(t)$	DI	$\sqrt{D\left(I^2+\frac{\Delta i_a^2}{12}\right)}$	$I+\frac{\Delta i_a}{2}$
D1	$i_{D1}(t)$		see $i_S(t)$	
	$u_{D1}(t)$	n.r.	n.r.	$\frac{U_a}{D}$
D2	$i_{D2}(t)$	$(1-D)I$	$\sqrt{(1-D)\left(I^2+\frac{\Delta i_a^2}{12}\right)}$	$I+\frac{\Delta i_a}{2}$
	$u_{D2}(t)$	n.r.	n.r.	$\frac{U_a}{D}$
C_a	$i_{Ca}(t)$	0	$\frac{\Delta i_a}{2\sqrt{3}}$	n.r.

table 2: relevant secondary side stress quantities

Determination of design parameters for the comparative analysis

Besides the already calculated stress-quantities applicant specific requirements should also be included, which mainly affect the output low pass filter.

These specifications and their influences are:

parameter		influences
$U_{imin,max}$	: DC input voltage range	Range of duty cycle D
I_{min}	: min. value of output current	cont. filter current $i_a(t)$ ⇒ value of L_1
$U_{awssmax}$	: max. output voltage ripple	
Δi_{max}	: max. step load	
Δu_{amax}	: Variation of output voltage at step load Δi_{max}	Value of L_1 and C_a
t_R	: settling time	

table 3: specific requirements

In order to fulfill these requirements the parasitic elements of the output capacitor cannot be further ignored. Therefore, besides the ideal output filter capacitor, a series equivalent inductance L_{ESL} and resistance R_{ESR} is considered by the following tabulated equations in table 4.

	single ended
steady state	$U_{awssmaxS} = \Delta i_a\left[R_{ESR}+\frac{L_{ESL}f_S}{D_{min}(1-D_{min})}\right]$ $L_{1S} = \frac{U_a(1-D_{min})}{\Delta i_a f_S}$
step load	$t_{RS} = \frac{\Delta i_{max}L_{1S}}{U_a\left(\frac{D_{maxreg}}{D_{max}}-1\right)} = \frac{\Delta i_{max}(1-D_{min})}{\Delta i_a\left(\frac{D_{maxreg}}{D_{max}}-1\right)f_S}$ $C_{aS} = t_{RS}\frac{\Delta u_{amax}-\sqrt{\Delta u_{amax}^2-(\Delta i_{max}R_{ESR})^2}}{\Delta i_{max}R_{ESR}^2}$ $R_{ESR} \le \frac{\Delta u_{amax}}{\Delta i_{max}}$
	double ended
steady state	$U_{awssmaxBr} = \Delta i_a\left[R_{ESR}+\frac{L_{ESL}f_S}{D_{min}(1-2D_{min})}\right]$ $L_{1Br} = \frac{U_a(1-2D_{min})}{2\Delta i_a f_S}$
step load	$t_{RBr} = \frac{\Delta i_{max}L_{1Br}}{U_a\left(\frac{D_{maxreg}}{D_{max}}-1\right)} = \frac{\Delta i_{max}(1-2D_{min})}{2\Delta i_a\left(\frac{D_{maxreg}}{D_{max}}-1\right)f_S}$ $C_{aBr} = t_{RBr}\frac{\Delta u_{amax}-\sqrt{\Delta u_{amax}^2-(\Delta i_{max}R_{ESR})^2}}{\Delta i_{max}R_{ESR}^2}$ $R_{ESR} \le \frac{\Delta u_{amax}}{\Delta i_{max}}$

table 4: general equations for specific requirements

approximations at steady state

- no voltage variation of the ideal output capacitor ($u_{Ca}(t) \approx const. \approx U_a$)

approximations at step load

- neglection of converter dead time
- regulation of positive step load with maximum allowable duty cycle $D = D_{max\,reg}$
- ideal step load $\Delta i = \Delta i\,\sigma(t)$

Comparative analysis and design of a 5V/100A SMPS

For all considered components of the high current circuits the comparative analysis shows differences with respect to component volumes and power losses.
The design and comparison follows under general conditions for all converter topologies under consideration. Among the general design aspects a concrete design example is worked out following equal specifications, see **table 5**. Especially for the desired miniaturization of SMPS a comparable design is of high significance.

$U_a = 5\ V$	DC-output voltage
$I = 100\ A$	output current
$I_{min} = 5\ A$	output current (min. value)
$D = 0.3$	duty cycle at $U_i = 300\ V$
$U_{imin} = 240\ V$	min. DC input voltage $\Rightarrow D_{max} = 0.38$
$U_{imax} = 375\ V$	max. DC input voltage $\Rightarrow D_{min} = 0.24$
$f_S = 100\ kHz$	switching frequency
$U_{awssmax} = 50\ mV$	max. ripple of output voltage
$\Delta i_{max} = 50\ A$	max. positive step load
$\Delta u_{amax} = 250\ mV$	variation of output voltage at step load Δi_{max}
$D_{max\,reg} = 0.45$	max. duty cycle at positive step load

table 5: converter specifications

a. power rectifiers

The power rectifiers on the secondary side of the transformer cause the dominant power losses of the power circuit.
Hence, their relevant stress quantities are discussed first. See **table 6**.

converter	rectif.	U_{DRmin}	I_{DAV}	I_{DRMS}	i_{Dmax}
forward	D_1	$\frac{U_a}{D}$	DI	$\sqrt{D\left(I^2+\frac{\Delta i_a^2}{12}\right)}$	$I+\frac{\Delta i_a}{2}$
two-trans.-forw.	D_2		$(1-D)I$	$\sqrt{(1-D)\left(I^2+\frac{\Delta i_a^2}{12}\right)}$	$I+\frac{\Delta i_a}{2}$
half bridge full bridge push pull	$D_{1/2}$	$\frac{U_a}{D}$	$\frac{I}{2}$	$\sqrt{\frac{1+2D}{4}\left(I^2+\frac{\Delta i_a^2}{12}\right)}$	$I+\frac{\Delta i_a}{2}$
Cuk	D	$\frac{U_a}{D}$	I	$\sqrt{\frac{I^2}{1-D}+\frac{1-D}{3}\Delta i_a^2}$	$\frac{I}{1-D}+\Delta i_a$

table 6: stress quantities for power rectifiers

The comparative analysis of rectifier stress is based on a rectifier, whose conducting state can be approximated by on-state voltage U_d and equivalent series resistance r_d.
The total conduction losses $P_{vD\,dtotal}$ - the sum of all secondary side power rectifier conduction losses - are nearly equal to the total losses $P_{vD\,total}$, if the transient- and reverse losses are neglected. Center column of **table 7** shows the approximated total losses $P_{vD\,total}$ under general conditions, while the ratios of on-state losses versus on-state losses of the forward-converter are listed in the right hand column, if $\Delta i_a^2 \ll I^2$.

converter	$P_{V\,D\,total}$	$\frac{P_{V\,D\,total}}{P_{V\,D\,totalS}}$
forward two-trans.-forw.	$U_d I + r_d I^2$	1
halfbr. fullbr. push pull	$U_d I + r_d I^2 \left(D+\frac{1}{2}\right)$	$1 + k_1\left(D-\frac{1}{2}\right)$
Ćuk	$U_d I + \frac{r_d I^2}{1-D}$	$1 + k_1 \frac{D}{1-D}$

table 7: total rectifier power losses

$$k_1 = \frac{r_d I^2}{P_{V\,D\,dtotalS}} = 1/\left(1+\frac{U_d}{r_d I}\right)$$

For a high value of the output current the influence of r_d increases. The paramter k_1 is displaced to the limiting value of one. For the whole range of duty cycle variation it holds that $D - 1/2 < 0$. The term $D/(1-D)$ is allways greater zero. To term it in another way it was found that an application of rectifiers with similar on-state characteristics in double clocked converter types leads to least power losses, while there are maximum power losses in the Ćuk converter.
On first sight this fact is made clear more conveniently in **figure 3**, in which $P_{vD\,total}/P_{vD\,totalS}$ is plotted versus duty cycle D with k_1 as parameter.

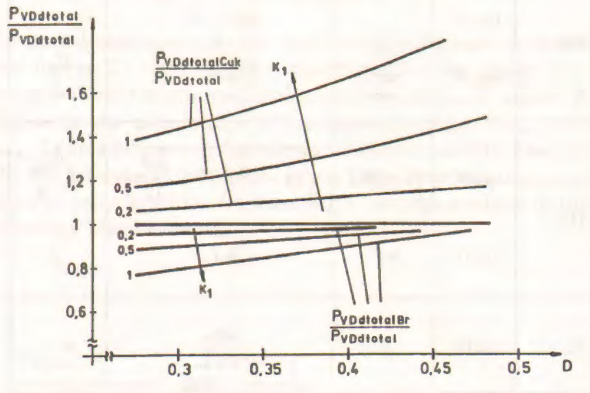

figure 3: normalized power rectifiers losses versus D

For the specified data ($D = 0.3, I = 100\ A$) and a Schottky diode with an equivalent on-state voltage $U_d = 0.4\ V$ and an equivalent resistance $r_d = 3\ m\Omega$ the following calculated results - see **table 8** - were attained with $k_1 \approx 0.43$.

converter	$P_{V\,Dtotal}$	$\frac{P_{V\,Dtotal}}{P_{V\,DtotalS}}$
forward two-trans.-forw.	70 W	1
halfbr. fullbr. push pull	64 W	0.91
Ćuk	83 W	1.19

table 8: total rectifier power losses for specified data

single ended converter	double ended converter
$L_{1S} = 4.6\ \mu H$ $t_{RS} \approx 20\ T_S$	$L_{1Br} = 1.6\ \mu H$ $t_{RBr} \approx 7\ T_S$
ETD 49 - core	ETD 39 - core
$N_S = 10$ $s_S \approx 5\ mm$ $P_{vS} \approx 8.5\ W$	$N_{Br} = 6$ $s_{Br} \approx 3\ mm$ $P_{vBr} = 4.2\ W$

table 9: design of smoothing choke L_1

with $P_{vS/Br}$: total power losses

b. choke L_1

The size of the smoothing choke is mainly determined by the ripple of the filter current $i_a(t)$. In addition to its effect on the dynamic response ($t_R \sim 1/\Delta i_a$) - as it follows from table 4 - the filter inductance is of importance for the output voltage ripple ($U_{aw..} \sim \Delta i_a$). In order to prevent discontinuous filter current mode the filter ripple current Δi_a should be large enough.
Common practise is to design the choke for minimum duty cycle D_{min}. This design criterion guaranties the demanded ripple current even for the worst case. The inductance ratio of double ended converters compared to single ended ones becomes:

$$\frac{L_{1Br}}{L_{1s}} = \frac{1-2D_{min}}{2(1-D_{min})}$$

In order to design the filter inductance select a common core (E,ETD,EF,RM etc.) and use the AP or KG approach /6/.

Design equations:

$$N_{S/Br} = \frac{L_{1S/Br} i_{amax}}{B_{max} A_e} \quad \text{with} \quad i_{amax} = I + \Delta i_a/2$$

$$s_{S/Br} \approx \frac{\mu_0 N_{S/Br} i_{amax}}{B_{max}} \quad \text{for} \quad s \gg \frac{le}{\mu_i}$$

with

A_e	:	effective cross - sectional area of core
B_{max}	:	max. allowable flux density
l_e	:	effective magn. path length
$s_{S/Br}$	:	air gap
$N_{S/Br}$	:	number of turns

Results for the mentioned example with the following additional design parameters are given by table 9.

additional design parameters:

$J_{max} = 5\ A/mm^2$	max. current density
$\varrho = 0.0232\ \Omega mm^2/m$	resistivity of conductor material
$U_a = 6\ V$	incl. secondary side DC-voltage drop
$B_{max} = 250\ mT$	
$\Delta i_a = 10\ A$	

The ETD 49 and ETD 39 core-parameters are given by data sheets. Suitable core materials are 3C8 by Valvo or N27 by Siemens for example.

c. output filter capacitor C_a

1. requirements for steady state

As to conclude from table 5 and based on the assumption, that the considered converter topologies show the same ripple current Δi_a. Two cases have to be distinguished:

a. The same output capacitor - first located in a single ended, second in a double ended topology - leads to:

$$U_{awssmaxBr} = U_{awssmaxS} + \frac{\Delta i_a L_{ESL} f_S}{(1-2D_{min})(1-D_{min})}$$

b. The same output voltage ripple:

$$U_{awssmaxS} = U_{awssmaxBr}$$

$$R_{ESRS} + \frac{L_{ESLS} f_S}{D_{min}(1-D_{min})} = R_{ESRBr} + \frac{L_{ESLBr} f_S}{D_{min}(1-2D_{min})}$$

For $R_{ESRS} = R_{ESRBr}$ we obtain: $\frac{L_{ESLBr}}{L_{ESLS}} = \frac{1-2D_{min}}{1-D_{min}}$

The results indicate, that the requirements for the parasitics are harder to fulfill in case of the double ended converter.

2. requirements for step load

As already mentioned C_a depends on the dynamics of the SMPS's. The termed formula for C_a gives different values for C_a whether the converter is single ended or double ended. If the same step loads are applied for all converter topologies, we get:

$$\frac{t_{RBr}}{t_{RS}} = \frac{(1-2D_{min})}{2(1-D_{min})} \quad \Rightarrow \quad \frac{C_{aBr}}{C_{aS}} = \frac{(1-2D_{min})}{2(1-D_{min})}$$

design of the output capacitor

The output filter capacitor has to fulfill electrical requirements for step load and steady state in respect of their parasitics.
The design procedure works iterativ and depends on the selected capacitor and its equivalent quantities.
For the design example based on those specifications of table 5 capacitors of type B 41 336 by Siemens with nominal voltage of 6.3 V were selected. Table 10 gives a review of the results obtained. The figures in brackets are due to the required ones by table 4.

value	single ended	double ended
C_a	$5 \times 10\ mF$ $(40\ mF)$	$6 \times 6.8\ mF$ $(14\ mF)$
R_{ESR}	$\approx 4\ m\Omega$ $(< 5\ m\Omega)$	$\approx 4.2\ m\Omega$ $(< 5\ m\Omega)$
L_{ESL}	$\approx 1\ nH$ (*)	$\approx 0.83\ nH$ (*)
$U_{awssmax}$	$\approx 42\ mV$	$\approx 42\ mV$
Δu_{amax}	$\approx 200\ mV$	$\approx 210\ mV$

table 10: design of output capacitor C_a

(*) the influence of L_{ESL} can be neglected

d. The secondary side located capacitor C_2 of Ćuk converter

Only the Ćuk converter requires a capacitor for power transfer, which in /4/ was said to be a good alternative to the common magneto-inductive way.
By neglecting the capacitor ripple voltage $\Delta u_{C2} \approx 0$ and the influence of the ripple currents Δi_a and Δi_2 ($I^2 \gg \Delta i_a^2, \Delta i_2^2$) the RMS-value of the capacitor current is given by:

$$I_{C2RMS} \approx \sqrt{\frac{D}{1-D}}\, I$$

Sticking to the prevailing example the capacitor has to withstand an RMS-value of 80 A for maximum load and a duty cycle $D = D_{max} = 0.38$.

Conclusion

The comparative analysis of the high current components of six selected converter topologies gives differences in component size and power losses or efficiency for the same specifications.
Regarding power rectifiers the resulting total losses for double ended converters are smaller than for the forward- and two-transistor-forward converter. In order to increase the efficiency of the Ćuk converter for high output currents one has to oversize the power diode. A possible advantage in terms of component count relative to rectifier is lost thereupon.
Volume and power losses of smoothing choke L_1 and output capacitor C_a for double ended converters compared with single ended converters are lower, too.

Therefore we summarize, that the double ended converters are the better choice to achieve higher power density, efficiency, lower weight and in respect of dynamics compared to single ended power converter by consideration of the secondary side located components only.
It should be noted that the high current RMS-value of capacitor C_2 forbids an application of the Ćuk topology at high current.

outlook

Besides the secondary side components the transformer and the components of the primary side (Power MOSFET's, input capacitor, input filter and bridge rectifier) have to be analyzed in comparison in order to complete a thorough investigation. Hence, to answer the question which converter is in favour of others to achieve the highest power density and lowest power losses depends on the whole power electronic circuits and extra circuitry for control electronics and gate drives.
The toughest problem in terms of mathematical analysis is due to the transformer. Only minimization of transformer losses (core losses, copper losses under consideration of Skin- and Proximity effects) and the leakage inductance will lead to a higher power density with increased switching frequency.

At present the analysis of the two winding transformer exited with various current waveforms is completed yet, but it is extended momentarily for a three- and four winding transformer and different, somehow exotic construction types for high output current in order to give final results about the comparison of the total power circuits.

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