Bachelors / Masters Thesis

X-aware Pattern Selection for Faster-than-at-Speed Test

Faster-than-at-Speed Test (FAST) is an approach to detect small delay faults, which can indicate an early life failure of a system. During FAST, the circuit under test is overclocked, which causes the simulation to generate more *unknown logic values (X-values)*, since some outputs did not finish their calculation at the target observation time (cf. figure 1). These X-values are a challenge for test response compaction, hence it makes sense to reduce these values as much as possible.

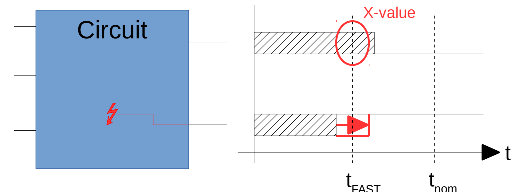

Figure 1: FAST generates X-values

One solution to reduce the number of X-values lies in selecting specific test patterns tuned to the target observation time. These patterns should produce only few X-values. There are already some methods to select patterns out of a base set, which are based on greedy and genetic algorithms.

Solution approach:

In this thesis, the method to select test patterns should be extended to further optimize the reduction in X-values. For instance, one could select special "essential" patterns, which produce a lot of X-values and replace them with newly generated patterns (by using a commercial pattern generator), optimized for FAST. For a Bachelors thesis, it is sufficient to check standard approaches (e. g. n-detect). For a Masters thesis, the essential patterns need to be analyzed further, such that the ATPG tool can be guided towards optimized patterns, e. g. by generating special constraints.

Solution aspects:

- Literature survey of the state of the art of FAST
- Find essential patterns which require replacement
- Generate new test patterns with a commercial tool
- Evaluate the method by means of simulation

Requirements:

- Interest in working in a current research topic
- Skills in C++
- **MA:** Passed "VLSI Testing" and "Introduction to Algorithms" (Only MA ESE)
- **BA:** Passed "Introduction to Algorithms" (Only BA ET), "Qualitätssicherung mikroelektronischer Systeme" is recommended

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Literature:

- S. Hellebrand, T. Indlekofer, M. Kampmann, M. A. Kochte, C. Liu und H.-J. Wunderlich, FAST-BIST: Faster-than-At-Speed BIST Targeting Hidden Delay Defects. Proceedings of the 2014 IEEE International Test Conference (ITC). Seattle, USA. Oktober 2014, pp. 1-8
- M. Kampmann, M. A. Kochte, E. Schneider, T. Indlekofer, S. Hellebrand and H.-J. Wunderlich, Optimized Selection of Frequencies for Faster-than-at-Speed Test. Proceedings of 24th IEEE Asian Test Symposium (ATS). Mumbai, Indien. November 2015, pp. 109-114