Real-time Digital Carrier & Data Recovery for a Synchronous Optical Quadrature Phase Shift Keying Transmission System

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***Abstract* — This paper focuses on the recent progress in coherent optical communication using advanced digital signal processing (DSP) technology. In particular the design of DSP components is presented which are required to realize a 10 Gbaud synchronous optical quadrature phase shift keying (QPSK) transmission system. Additionally the measurement results of a preliminary synchronous QPSK transmission setup with distributed feedback (DFB) lasers and real-time digital in-phase and quadrature (I&Q) receiver at a data rate of 1.4 Gbit/s are shown. The minimum bit error ratio (BER) was $1.7 \cdot 10^{-5}$, lower than ever reported before for a real-time system with DFB lasers.**

***Index Terms* — Optical communication, quadrature phase shift keying, synchronous detection, real time systems, digital integrated circuits.**

I. Introduction

Coherent optical communication, especially synchronous QPSK transmission, is attracting more and more attention because it can increase the spectral efficiency and the robustness against chromatic and polarization mode dispersions in high-capacity wavelength-division multiplex (WDM) transmission systems. Ultimate optical signal-to-noise ratio (OSNR) performance is promised by synchronous demodulation, which for QPSK outperforms the asynchronous or interferometric one by >2 dB, even if DFB lasers are employed. Indeed it was shown that ultra-narrow linewidth lasers are required to realize an optical phase locked loop (PLL) [1], and these lasers are believed to be too costly for standard commercial applications. However the PLL is dispensable if a feedfoward carrier recovery scheme is applied, which relaxes the sum linewidth requirement to 0.001 times the symbol rate. This is in the reach of standard DFB lasers [2]. A multitude of offline QPSK experiments with data rates from 20 Gbit/s to 86 Gbit/s [3][4][5] and first real-time experiments with lower data rates [6][7][8] already showed the potential of this technology.

However, to realize a real-time optical synchronous QPSK transmission system with a digital I&Q receiver at 10 Gbaud, high-capacity DSP components are required, which are not yet available on the market. This paper presents latest achievements in the DSP component development for a 10 Gbaud synchronous optical QPSK transmission system. Additionally, the experimental results of a preliminary testbed with a data rate of 1.4 Gbit/s are presented. In this test bed a BER of $1.7 \cdot 10^{-5}$ was achieved, the lowest BER ever reported for a real-time synchronous QPSK system with DFB lasers.

II. The European synQPSK project

The project "synQPSK – Key components for synchronous quadrature phase shift keying transmission", funded by the European Commission, aims at the realization of all key components which are not commercially available for the implementation of a 40 Gbit/s synchronous optical return-to-zero (RZ) QPSK transmission system with polarization division multiplex. The 3 year project was started in July 2004. The consortium consists of two industrial partners and two universities. Photline Technologies (France) develops a novel Lithium-Niobate ($LiNbO_3$) based QPSK modulator [9]; CeLight Israel fabricates a 90° optical hybrid in $LiNbO_3$ technology [10]. The Univ. Duisburg-Essen (Germany) develops Indium-Phosphite (InP) based balanced photoreceivers which will be co-packaged with CeLight's 90° optical hybrids; and the Univ. Paderborn (Germany) designs the signal processing components [11] and develops the system testbed. The target system of the synQPSK project is shown in Fig. 1.

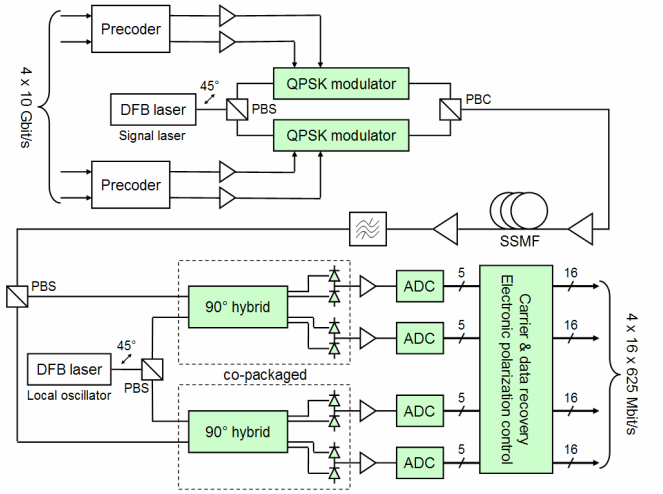

Fig. 1. Target system for 40 Gbit/s synchronous optical QPSK transmission with polarization division multiplex (new components under development are inked).

Synchronous QPSK transmission combined with RZ coding and polarization division multiplex is an extremely attractive modulation format for metropolitan area and long haul fiber communication. Compared to standard intensity modulation the line rate is 4 times lower, the needed number of photons per bit is less than half as high, the tolerance to chromatic dispersion and polarization mode dispersion several times better, and the tolerance against fiber nonlinearities, in particular cross phase modulation, is substantial. Moreover, the detected electrical signals are proportional to optical fields. This transfers the advantages of photonic processing 1:1 into the electrical domain. In particular, all linear optical distortions such as polarization transformations, polarization mode dispersion (PMD) or chromatic dispersion (CD) can be equalized electronically without losses. Synchronous QPSK possesses also distinct advantages over all other phase modulation formats, in particular duobinary, differential phase shift keying (DPSK), differential quadrature phase shift keying (DQPSK) and all variants thereof.

III. DSP COMPONENTS FOR REAL-TIME CARRIER & DATA RECOVERY

In the following the DSP components are described that are being developed inside the synQPSK project. These components are essential for the realization of a 10 Gbaud synchronous optical QPSK transmission system.

A. Analog-to-digital converter

The synchronous QPSK receiver requires a very fast analog-to-digital converter (ADC) with a sampling rate of 10 GSamples/s (Gs/s) or up to 12.5 Gs/s in case of forward error correction (FEC) to be able to digitize the incoming 10 Gbaud QPSK signal. A very good architecture for such high-speed ADCs is the full-flash topology where 2^N-1 parallel comparators are utilized to digitize the signal with a resolution of N bits in one step. The practical resolution is limited to 4 – 6 bits due to the loading of the input buffer with the 2^N-1 comparators and restricts the achievable bandwidth and sampling speed. Table 1 shows the specifications of the ADC developed for the synQPSK project.

TABLE I - SPECIFICATIONS OF THE ADC

Technology	0.25 µm SiGe:C BiCMOS
Resolution	5 bit
Sampling rate	> 15 Gs/s
Effective number of bits (at Nyquist frequency)	4.5 @ 15 Gs/s
Signal-to-noise-and-distortion ratio (SINAD) (at Nyquist frequency)	28.9 dB @ 15 Gs/s
Full scale range (V_{FSR})	500 mV
Power consumption	4.3 W
Supply voltages	-4 V; +1.8 V
Number of transistors	3296
Chip size	6.4 mm^2

A very fast circuit technology is necessary to accomplish the required sampling rate of >10 Gs/s, together with a fairly high level of integration to incorporate the encoding stages of the ADC. A 120 GHz SiGe hetero bipolar technology (IHP, Germany) was sufficient to achieve the desired sampling rates. A chip photograph of the 5 bit ADC is depicted in Fig. 2.

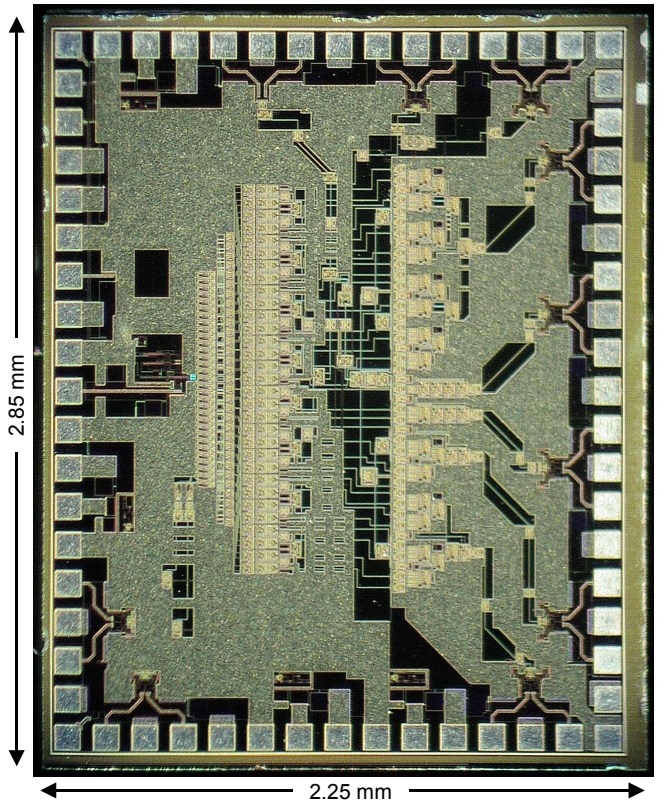

Fig. 2. Photograph of the 5 bit SiGe ADC chip.

B. Digital signal processing unit

To facilitate the signal processing functions for the carrier recovery and polarization control a standard-cell based silicon CMOS technology is preferable due to its higher integration capability and lower power requirements compared to a bipolar technology. A drawback of CMOS standard-cell design is the limitation of the attainable data rates. Therefore, a fast demultiplexer must be build into the DSP unit to allow a high speed interface with the 10 Gbit/s input signals from the ADC. It is realized with a full-custom 1:8 demultiplexer circuit, integrated together with the standard-cell design into a single chip. The full-custom demultiplexer uses a differential circuit topology (source coupled FET logic) to achieve the necessary data rates for the high speed interface.

The standard-cell based DSP unit further demultiplexes the internal data stream to 625 Mbit/s to enable complex processing and performs the carrier & data recovery in 16 parallel units in a PLL-free approach [11]. At the output of the

TABLE II - SPECIFICATIONS OF THE CMOS CHIP

Technology	120 nm CMOS
Data input (differential)	2 x 5 bit
Input amplitude (single ended, 50 Ω)	400 mV
Input sampling rate	1 – 10 Gs/s
Input clock frequency	0.5 – 5 GHz
Supply voltages	+1.2 V, +1.8 V, +3.3 V
Number of gates (DSPU)	63,187
Number of transistors (full-custom DeMux)	5,145
Power consumption @ 10 Gbit/s	~1.2 W
Chip size	7.2 mm^2

DSP unit 32 recovered data bits (16 channels, I&Q) are available at a data rate of 625 Mbit/s.

Table 2 lists the specifications of the combined full-custom demultiplexer and the standard-cell DSP unit using a 120 nm CMOS technology from ST Microelectronics (France) with a f_T = 90 GHz and a threshold voltage V_T = 0.3 V.

The first version of the chip does not support polarization division multiplex and automatic polarization control, but it will be included in the next chip design currently under development. Fig. 3 shows the photograph of the CMOS chip.

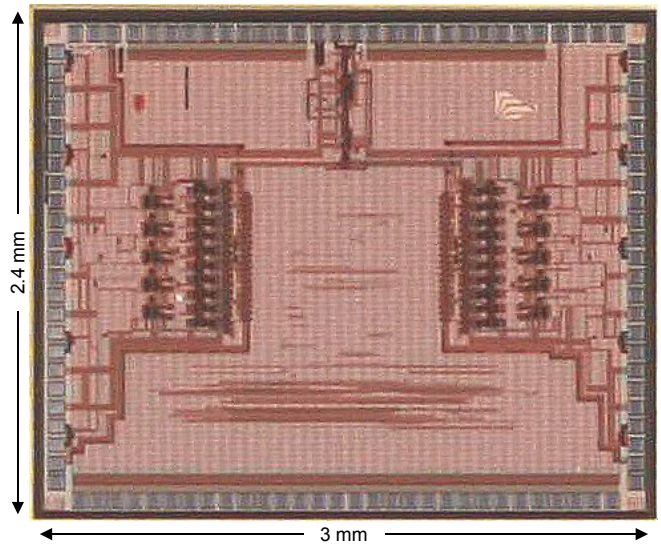

Fig. 3. CMOS chip with combined full-custom design for demultiplexing and standard-cell design for carrier & data recovery.

IV. PRELIMINARY EXPERIMENTAL RESULTS FOR SYNCHRONOUS OPTICAL QPSK TRANSMISSION WITH COMMERCIALLY AVAILABLE DSP COMPONENTS

A. Experimental setup

The transmitter uses a DFB signal laser and a QPSK modulator driven with 2x700 Mbit/s PRBS data (Fig. 4). Normally the I&Q data is Gray-encoded to form a quadrant number, which is modulo 4 differentially encoded to determine the quadrant of the optical phase. In this setup, identical PRBS are used as I&Q modulator driving data, mutually delayed by 7 symbols for decorrelation, and differential quadrant encoding is not implemented. To take this omission into account and to enable BER measurements, appropriate bit patterns are programmed into the BER tester (BERT).

After transmission through 63 km of standard single mode fiber, the signal is optically preamplified and filtered by a ~20 GHz wide bandpass. In addition a polarizer (not shown) reduces receiver overloading by wideband amplified spontaneous emission. The coherent receiver features a second DFB laser as its local oscillator, and manual polarization control. The two optical signals are superimposed in a $LiNbO_3$ 90° optical hybrid and detected with two photodiode pairs. The resulting electrical I&Q signals are amplified before being sampled in 6 bit ADCs.

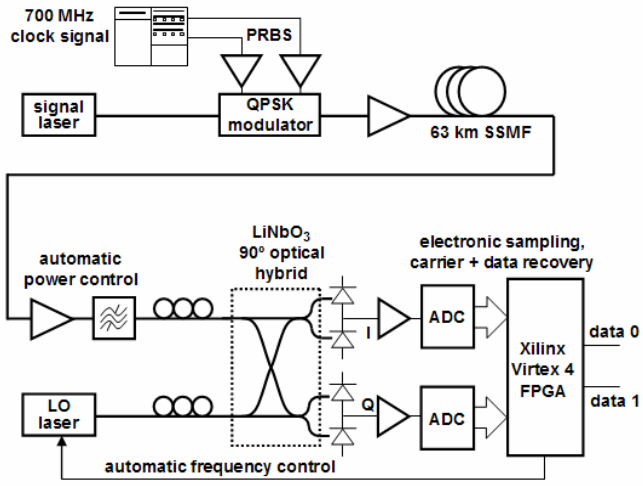

Fig. 4. 1.4 Gbit/s preliminary QPSK transmission setup with real-time synchronous coherent digital I&Q receiver.

The ADCs interface with a Xilinx Virtex 4 FPGA where electronic carrier and data recovery is implemented [12]. The data recovery includes a differential modulo 4 decoding of the received quadrant number, to prevent occurring quadrant phase jumps of the recovered carrier from falsifying all subsequent data. Most processing occurs in parallel units at a rate which is 16 times lower than the symbol rate. The results of every fourth unit are re-assembled to form sequential I&Q bit streams whose BERs are measured and averaged.

B. Measurement results

The 3 dB sum linewidth of the DFB lasers (JDSU) is specified as $\Delta f \leq 2$ MHz. The measured heterodyne spectrum contains sidelobes 30 dB down at ±30 MHz. They are most likely caused by reflections and can degrade system performance. Fig. 5 shows the averaged measured BER vs. optical power at the preamplifier input of the receiver after transmission over a distance of 63 km. The best measured BER for a data rate of 1.4 Gbit/s was $1.7 \cdot 10^{-5}$, and was constant

when the preamplifier input power was higher than -37 dBm. The recovered bit streams could be synchronized to the expected patterns until the preamplifier input power was set below -51 dBm.

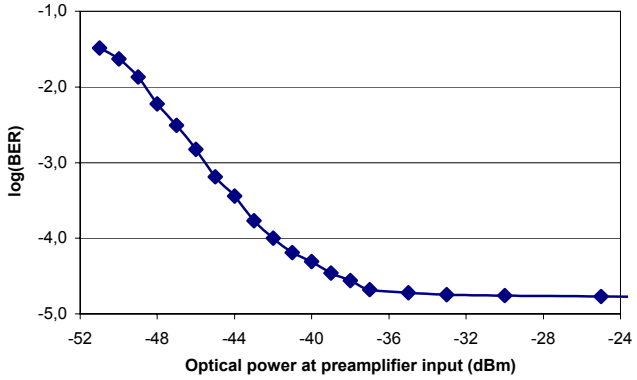

Fig. 5. Measured BER (I&Q averaged) vs. optical power at the preamplifier input at 1.4 Gbit/s data rate.

C. Discussion

A FEC coding scheme with 7% overhead is able to recover (quasi) error-free data for a raw BER below 0.1%. Our 1.4 Gbit/s QPSK transmission therefore corresponds to an error-free data rate of 1.3 Gbit/s, assuming the presence of such an FEC.

For various data rates, BER floor values are plotted as a function of the product of sum linewidth and symbol duration T (Fig. 6). The floor drastically drops when T is reduced. Very good performance with standard DFB lasers can be achieved at 10 Gbaud, which corresponds to 20 Gbit/s data throughput, or even 40 Gbit/s with additional polarization multiplex.

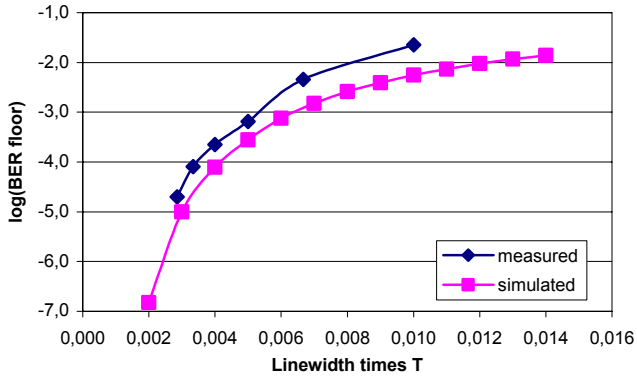

Fig. 6. BER floor for different products of sum linewidth times symbol duration T. Measured data refers to a nominal $\Delta f = 2$ MHz.

V. Conclusion

We have presented the design for the DSP components required to realize a 10 Gbaud synchronous optical QPSK transmission system. Additionally we have demonstrated synchronous QPSK transmission using commercially available DFB lasers and a real-time digital receiver. 1.4 Gbit/s QPSK data was transmitted over 63 km with FEC compatible performance and a minimum BER of $1.7 \cdot 10^{-5}$. To our knowledge, this is the lowest BER ever reported for a real-time QPSK transmission system with DFB lasers.

Acknowledgement

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