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Master Project

Design and Development of a Drive Inverter for Racing Applications

by

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Filing Date: April 14, 2024

Abstract

In this thesis, the electronic hardware of a drive inverter for racing applications of the UPBracing Team with Silicon Carbide power switches according to the Formula Student Germany Regulations 2024 v1.1 is designed and developed. In addition to the conceptual design of the overall system and its adaptation to the existing vehicle environment, the main focus here is on the development of the power electronics part and the insulation interface between the high-voltage drivetrain system and the low-voltage control system. The development focuses on a maximum cost effective, lightweight and small system design. As a comparative reference, a purchased inverter system, which was installed in each UPBracing Team's electrical race car since 2019, is used. The selection of crucial components, such as the power switches or DC link capacitors, is based on previous analytical estimations for the expected power losses of the switches and a current ripple analysis for the DC link capacitors. Also three different power loss analysis methods are compared in view of computation time, computation effort and accuracy.

Contents

1 Introduction

In recent years, the trend has shifted toward electric vehicles. In 2022, the European electric vehicle market has shown a steady increase in registrations over the years, reaching a significant milestone in 2022. Electric vehicles accounted for 21.6 % of new car registrations, up from 18 % in 2021. [1]
In addition to that, in the final quarter of 2023, the United States set a new record with fully electric vehicles capturing an 8.1 % share of the market. This achievement represents a notable rise from the 6.5 % market share recorded during the same timeframe in 2022. Furthermore, for the first time in 2023, electric vehicle sales in the United States exceeded one million units, reflecting an increased interest and investment in electric mobility. [2]
Electromobility also found its way into motorsport through the introduction of the all-electric Formula E racing series in 2014 [3]. In addition to the long-established racing series, Formula E also serves as a platform for research and development activities relating to electric vehicles in order to test the latest electric technology for future road cars [4].
Another branch of motor racing that also relies more heavily on fully electrical race cars is the Formula Student, a unique and reserved racing class for students. Here, students can gain experience in design and production in the automotive industry [5]. In the future for instance the most famous and most competitive Formula Student event, Formula Student Germany at the Hockenheimring, will only allow all-electric race cars to compete from 2024 onwards, thus cancelling the combustion class completely [6]. These changes in the regulation and plans for the future of Formula Student Germany have a big impact on the Formula Student teams, too. Because the main difference between combustion and electric vehicles lies within the drive train, the most complex part of a race car needs to be newly developed from scratch.
An important and necessary component in battery electric vehicles is the drive inverter, which, together with electrical motors, makes it possible to move the car. The exact task of such a drive inverter is to convert the direct current from the traction system's battery into individual alternating currents for each motor, depending on the actual torque and speed command generated from the driver respectively the vehicle dynamics control while offering the opportunity to continuously monitor the temperatures and currents of the motor and the drive inverter itself to protect the traction system from damage by internal derating or setting the race car back in a safe state, if unavoidable.

1.1 Motivation

Driven by the global trend of battery electric vehicles and the conversion of the Formula Student competition to fully electric race cars, the UPBracing Team decided in 2019 to build its first electrical race car prototype and to continue building only battery electric vehicles in the future. Since the development of a fully electric car comes with a huge effort in designing the electrical system, the UPBracing Team has been using purchased inverters until now to reduce the design effort and to first focus on the development of components where purchased parts are not a suitable alternative, such as the traction system's battery along monitoring system, as well as the general low voltage and safety electronics, to ensure that a fully functional race car can be completed within one year.
During the last five years, the UPBracing Team continuously enhanced the robustness and reliability of the traction system's battery, its monitoring system, and the low-voltage electronics. Therefore, no big improvements are expected to be made in the next seasons. But to be more independent of pre-designed systems from the industry, the next step is to replace the purchased drive inverter system with an in-house developed solution. This allows the UPBracing Team to customize the inverter assembly more to its needs thus reducing the weight and size of the drive inverter package while gaining the overall system's performance and efficiency.

1.2 Objectives

As the design and development of an inverter, beginning with the definition of requirements and selection of suitable components, continuing with hardware layout and assembly, implementing the motor control, final testing and optimizing the whole system is a big effort, this thesis focuses on the first stages of such a design process and sets the basis for further development steps. Especially the definition of requirements based on the Formula Student Germany Regulations 2024 v1.1 respectively requests of the UPBracing Team and the high-voltage power electronics hardware development are covert.
The selection of suitable power electronic components, in particular Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), is supported by power loss analyses and thermal simulations. Also included is a comparison of different power loss estimation methods for drive inverter designs. The operating region for the MOSFETs, and with this the simulation parameters, are derived from the specifications of the electric motor, which will be used in the future by the UPBracing Team. Additionally, the system is responsible for keeping itself and the motors in a safe operating region and to re-enter the safe state in case of a failure. The interface to the car is already defined by the existing inverter and is considered in the design phase. To limit the complexity of the drive inverter design, a single inverter for the operation of only one electric motor is developed. The system can easily be expanded to four of these individual inverters to operate all the wheels of a race car independently of each other later on.

2 Theoretical Background and Basics

In the following the definitions and the wording of the Formula Student Regulations 2024 v1.1 are summarized. Additionally, the operating principle of an electric motor is explained, in particular of a Permanent Magnet Synchronous Motor (PMSM) as the UPBracing Team only uses PMSMs. After that the need for a drive inverter is derived and its operating principle is described. Based on this the power loss estimation methods for the power switches are then dealt with. Besides this, a calculation method for a rough estimation of the necessary Direct Current (DC) link capacitance is presented.

2.1 Definitions in Formula Student

Almost all European Formula Student events in 2024 take place by the generally applicable Formula Student Germany Regulation 2024 v.1.1 (see [7]). The definitions of the regulation relevant to this thesis are summarized below. Every regulation relating to the maximum occuring drivetrain voltage of the race car is simplified for $600\,\mathrm{V_{DC}}$, since the $7.6\,\mathrm{kWh}$ big battery, which serves as the energy storage for the drivetrain of the race car, has a voltage of $600\,\mathrm{V_{DC}}$ when it is fully charged.

2.1.1 Tractive System

The Tractive System (TS) is defined as every part that is electrically connected to the TS accumulator or the motors. The maximum allowed system voltage of the TS is limited to $600\,\mathrm{V_{DC}}$ between any two electrical connections. For inverter internal low power control signals, the permitted voltage between any two electrical connections is increased to $630\,\mathrm{V_{DC}}$, e.g. for the gate drivers and their power supplies of the high side switches.

2.1.2 Low Voltage System

The Low Voltage System (LVS) is therefore any electrical part, that is not part of the TS, i.e. is not connected to the TS accumulator or the motors.

2.1.3 Galvanic Isolation between Tractive System and Low Voltage System

TS and LVS must be galvanically isolated. The isolation resistance must be at least 300 kΩ. All components that work as the isolation barrier must have an isolation test voltage rating of at least 1800 $V_{RMS,AC}$ for one minute and the specified working voltage must be higher than 600 V_{DC}.

2.1.4 Spacing between Tractive System and Low Voltage System

TS and LVS must always be separated. On a Printed Circuit Board (PCB), TS and LVS must maintain a spacing of at least 4 mm if the conformal coating is applied. Without conformal coating but with a cutout in the board between the TS and LVS areas, the minimal permitted spacing is increased to 9.5 mm. Without conformal coating or a cutout, a minimum distance of 12.7 mm is required.
TS and LVS components within one enclosure must maintain a minimum spacing of 30 mm or must be separated by a moisture-resistant insulating barrier. TS and LVS areas on one PCB are considered as a single TS respectively LVS component.

2.1.5 Electrical Connections

Each electrical connection in the high current path of the TS must be secured against unintentional loosening. Fasteners must be secured by either safety wiring, cotter pins, prevailing torque lock nuts, locking plates, or tab washers. Soldered connections in the high current path are only permitted if it is a connection to a PCB, no connection to wires, and when the component is additionally secured against unintentional loosening.

2.1.6 Safe State

The safe state is present when the TS battery is electrically not connected with the vehicle and the voltage across the DC link capacitance is below 60 V. There is no special requirement for the motors to be free of torque, as no torque can be generated by the motors if the inverter is disconnected from the TS battery, its power supply.

2.1.7 System Critical Signal

For each analogue System Critical Signal (SCS), e.g. the indication signal for a voltage of more than 60 V across the DC link, a short circuit to ground or supply voltage, an open circuit and an implausibility due to out-of-range signals must be detected and must result in the safe state of the race car.

2.1.8 Shutdown Circuit

The Shutdown Circuit (SDC) directly conducts the power to establish the electrical connection between the TS battery and the vehicle. It consists of a series connection of switches which can open the SDC and thus prevent an electrical connection between the TS battery and the vehicle. When the SDC is opened, the voltage across the DC link capacitance must drop below 60 V within 5 s. All switches which can open or close the SDC must be designed in a way, that the SDC is opened in a deenergised condition. All signals influencing the SDC are SCS. To reach the safe state, the SDC needs to be opened.

2.1.9 Tractive System Active Light

The Tractive System Active Light (TSAL) indicates the TS status and is mounted on the mainhoop above the driver's head. If the TS is active, so the voltage across the DC link capacitance is equal or greater than 60 V, the TSAL must have a red flashing light. Therefore, the inverter must signal a DC link voltage of over 60 V to the car. Signals influencing the TSAL are SCS.

2.2 Operating Principle of a Permanent Magnet Synchronous Motor

The operating principle of a PMSM is based on the interaction between a Rotating Magnetic Field (RMF) generated by the stator and a magnetic field generated by permanent magnets on the rotor. Contrary to the case of induction motors in which the rotor magnetic field is induced by the winding of the stator, permanent magnet synchronous motors have permanent magnets embedded in the rotor to produce a constant magnetic field. [8]

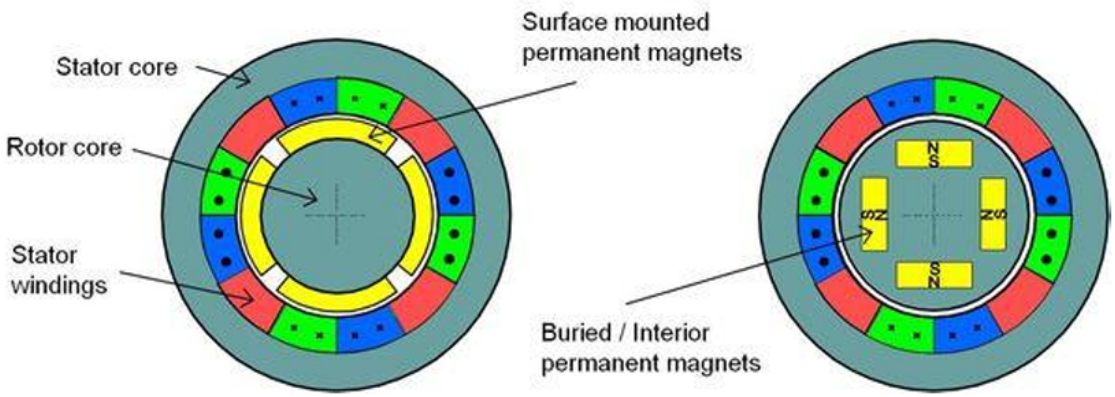


Fig. 2.1: Internal depiction of a PMSM [8]

Fig. 2.1 depicts the inside of a general PMSM. Torque is produced when the two magnetic fields from the rotor and stator interact which results in the movement of the rotor. The movement is a rotation synchronous to the frequency of the RMF of the stator. This means the rotor moves at a speed equal to the RMF of the stator. Whereas, the speed of rotation of the magnetic field of the stator depends upon the frequency of the supply and the number of poles present in the stator. Since PMSMs have the potential to provide a high output torque to stator current ratio, i.e that for a given amount of electric current PMSMs can produce more torque compared to other types of motors, high power-to-weight ratio, and robustness, they are ideal for the use of variable-speed Alternating Current (AC) drives, and even more specifically in the case of electric vehicles [9].

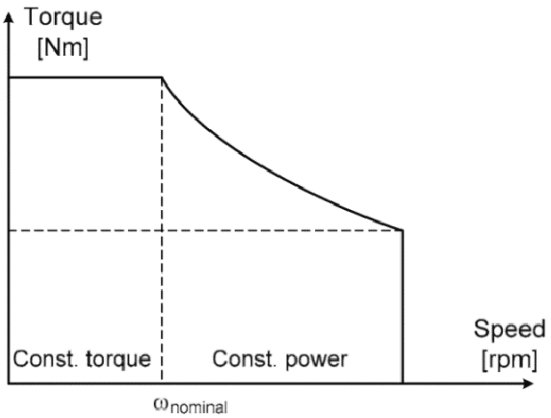


Fig. 2.2: Ideal torque-speed characteristics of a PMSM [10]

Fig. 2.2 is a graphical explanation of the torque-speed characteristics of PMSMs that are known to be able to work in the overspeed range. This means that the real speed of the motor can exceed the nominal speed. However, to increase the speed above the rated speed the flux should be reduced while the voltage is to be kept constant. For this purpose, it is essential to control the current such that the stator current (i_{sd}) in the direct axis (the axis aligned with the rotor's magnetic field direction) is adjusted appropriately, and the current in the quadrature axis (axis perpendicular to the direct axis) path is maximized. The torque is inversely proportional to the speed, so the output power remains constant for the range where the rated speed is exceeded. [10]

2.3 Operating Principle of an Inverter

An inverter can be roughly divided into two units, the power electronics and the control unit. The power electronics can again be split into two subgroups. One is the inverting stage, which consists of six switches in the case of a three-phase two-level inverter, which is used by the UPBracing Team and generates the needed AC phase currents for the motor. The second subgroup is the DC link capacitance, which is connected very close to the DC input side of the inverting stage. The control unit controls the power electronics and monitors the state of the motor and the inverter itself.

2.3.1 Inverting Stage

The three-phase two-level inverter converts the supplied DC voltage into three AC voltages depending upon the switching patterns of the switches in the inverting stage. This drive inverter design uses SiC MOSFETs as switches. The switching patterns are determined by the control unit, which generates Pulse Width Modulation (PWM) signals that are amplified by gate drivers and fed to the gates of the MOSFETs. However, this means that, unlike a regular inverting system, the drive inverter can generate a frequency variable AC power by varying the switching patterns of the MOSFETs.

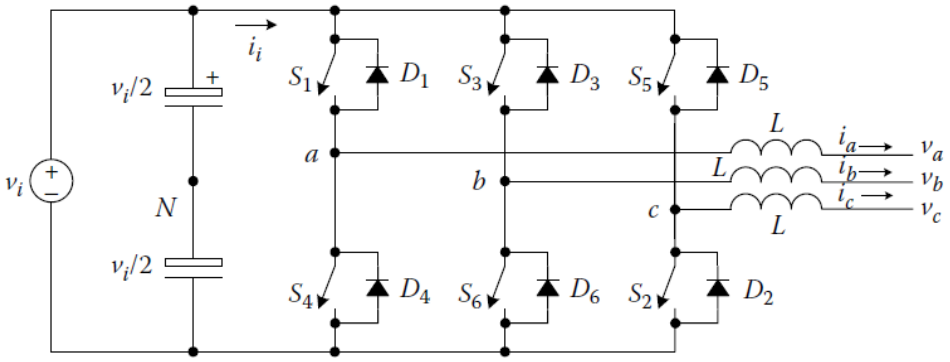


Fig. 2.3: Three phase two level voltage source inverter [11]

Fig. 2.3 depicts a three-phase two-level voltage source inverter. The inverter operates in eight switching states while two switches of the same leg cannot be closed simultaneously since it would short the input voltage. The advantage and purpose of using such a topology is to provide a three-phase voltage supply in which the amplitude, phase, and frequency can be controlled.

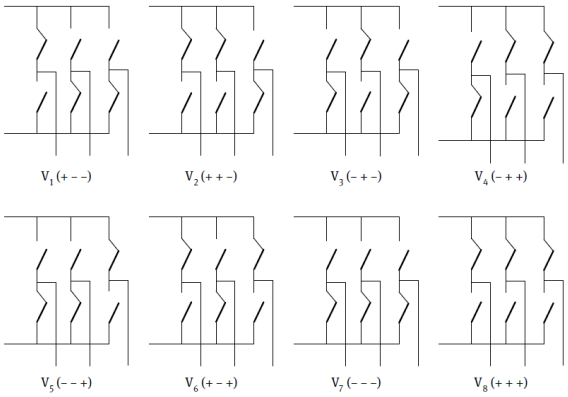


Fig. 2.4: Switching states of a three phase two level inverter [12]

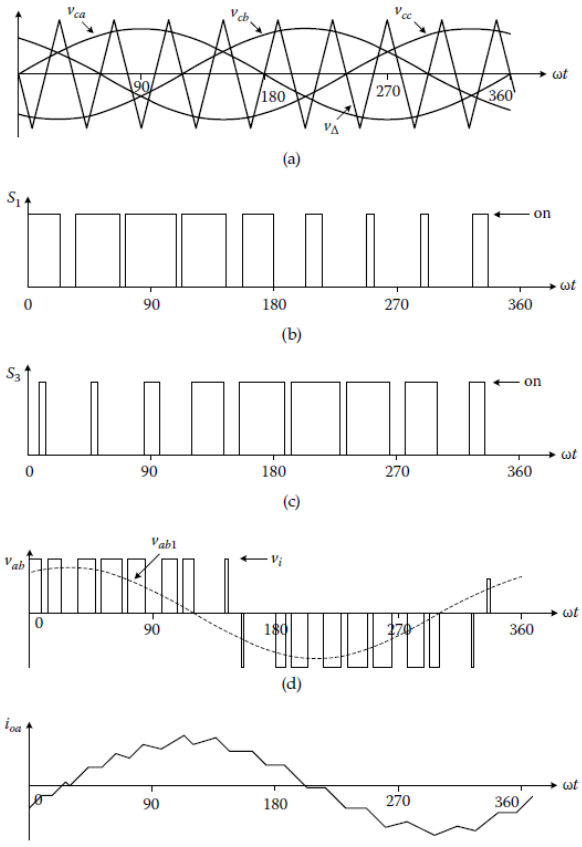


Fig. 2.5: Inverter waveforms [11]

Fig. 2.4 depicts the eight switching states of the inverter. The resulting voltage waveform from these states is visualized in Fig. 2.5(d) for one phase.

2.3.2 Control Unit

The control unit of the system is responsible for communication with the race car and for safe operation of the inverter. A bidirectional communication via Controller Area Network (CAN) is necessary to receive the torque command τ^* and the speed command ω^* from the vehicle control unit and to transmit system status information like the actual torque τ, actual speed ω, inverter temperature ϑ_{Inv}, motor temperature ϑ_{Mot} and the phase currents $i_{\mathrm{sa,b,c}}$. In the event of overtemperature, overcurrent or detected component failure, the controller should stop the PWM signal generation and make the car reach the safe state, defined in section 2.1.6.

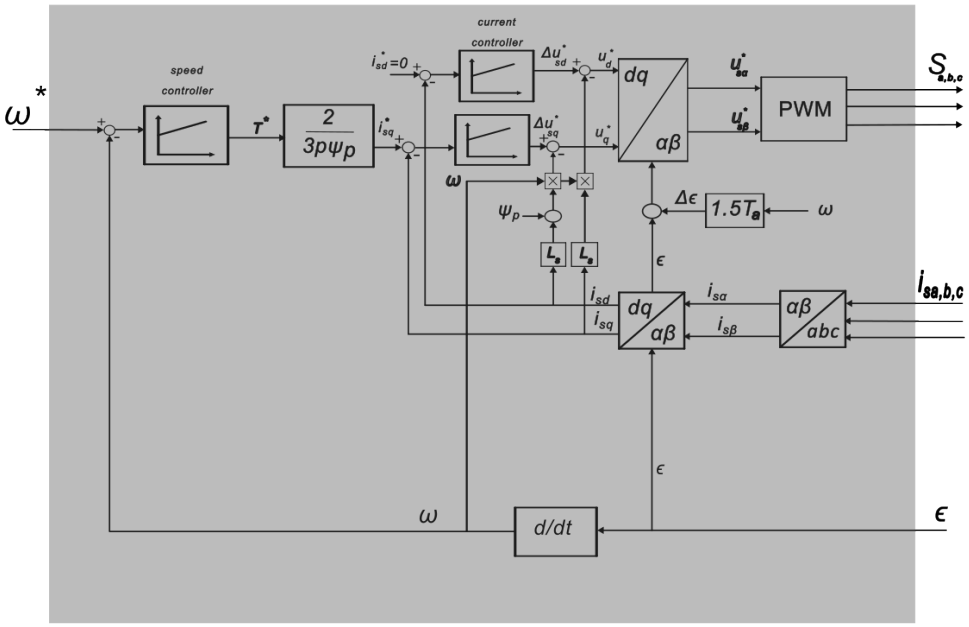


Fig. 2.6: Controller block diagram

Fig. 2.6 depicts the motor controller part of the control unit in a block diagram. The grey area represents the motor control loop, which is implemented in software on a microcontroller, but whose implementation is not part of this project. However, the block diagram clearly shows which input signals are required to control a motor and which output signals are provided. In detail the input signals are the requested motor speed setpoint ω^*, the phase current signals $i_{\mathrm{sa,b,c}}$ and the rotation angle of the rotor ϵ respectively the rotor speed ω as the time derivative of the rotor's angle ϵ. The PWM signals $s_{\mathrm{a,b,c}}$ are the only outputs of the motor control part of the control unit.
To relieve the motor controller, an additional processor can overtake safety-critical tasks like the detection of component failures or overcurrent events. This is especially advantageous, as the motor controller is often too slow for such time-critical protection measures or even could lead to a fault. [13]

2.4 Selection of Crucial Components

To select proper components, some analytical estimations were done before the design process. This belongs especially to the DC link capacitance and the SiC power switches.

2.4.1 DC Link Capacitor

The DC link capacitance is an important component in power electronic systems such as converters, inverters, power supplies, and variable frequency drives. The DC link capacitance is based on one or a group of capacitors that are sat in between the supply voltage and the plant of the system or/and between the output and plant of the system (can be the inverter bridge, rectifier bridge, etc). This is done to reduce and eliminate the voltage ripples which ensures a smooth DC supply.
Apart from the above, the DC link capacitance can be attributed to the following functions as well:

- Temporary energy storage for dynamic conditions to ensure a consistent voltage supply (at the input for the inverter, in this case) and by doing so avoiding disturbances and degradation in the system's performance.
- Acting as a buffer and protecting from the sudden voltage surge to the other components in the circuit.
- Compensating for parasitic inductance in long lines (tracks, wires etc).

The minimum necessary capacitance for the DC link of a drive inverter system can be calculated according to [14] with the following equation:

$$C_{\mathrm{DC,min}} \geq \frac{\Delta P_{\mathrm{max}} \cdot T_{\mathrm{sw}}}{2 \cdot V_{\mathrm{DC}} \cdot \Delta V_{\mathrm{DC}}} \tag{2.1}$$

where:

- T_{sw} is the switching period
- ΔP_{max} is the maximum power variation of the inverter in one switching period T_{sw} (e.g. a load step of twice the rated nominal power, which occurs at startup with operation at the current limit)
- ΔV_{DC} is the maximum allowable voltage fluctuation (around 10 % of the DC link voltage V_{DC})

Since a two-level drive inverter generates an alternating output current by switching between two voltage potentials, the DC link capacitors also experience current ripples due to the switching behavior. Therefore, the capacitors should be rated for the occurring current ripple. To quickly estimate the current ripple I_{ripple}, the following formula can be used, which was derived in [15]:

$$I_{\text{ripple}} = \hat{I}_{\text{max}} \cdot \sqrt{M \cdot \left(\frac{\sqrt{3}}{4 \cdot \pi} + \cos^2(\varphi) \cdot \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} \cdot M \right) \right)} \tag{2.2}$$

Here, M represents the Modulation Index and $\cos(\varphi)$ the Power Factor of the operating point respectively φ the angle between voltage and current.

2.4.1.1 Comparison and Types of Capacitor for DC Link

There are various types of capacitors used for DC link. Some common types are as follows:

- Aluminium electrolytic capacitors
- Polypropylene film capacitors
- Ceramic chip capacitors

2.4.1.2 Aluminium Electrolytic Capacitors

Electrolytic capacitors are based on the use of electrolytes to have higher capacitance than other capacitor types. Electrolytic capacitors are generally polarised, meaning that the positive terminal is always on a greater potential than the negative terminal of the capacitor. Electrolytic capacitors can be made of either wet-electrolyte or solid polymer. [16]

The wound cell of the electrolytic capacitors is the active part and consists of aluminum (anode and cathode foil) paper and electrolyte. The electric current flow in this type of capacitor is made possible due to the ions flowing through the electrolyte, therefore the viscosity of the electrolyte acts as an important factor for the temperature dependence of the Equivalent Series Resistance (ESR). For low temperatures, the electrolyte is more viscous and thus allows a free flow of the ions, increasing the ESR. However, the capacitance is also affected by falling temperatures. In addition to that, the frequency dependence for capacitance and ESR is also strong. [17]

The voltage rating of such capacitors is limited to 650 V in many cases. Therefore due to the voltage and ripple current limitations of a single electrolytic capacitor multiple capacitors in series and/or in parallel are used to create a "capacitor bank". However, by a series connection of multiple capacitors, a balancing circuit is required to ensure, that all capacitors are equally charged and thus have the same voltage. Otherwise, an imbalance can occur, which in the worst case can lead to only one capacitor being fully charged and the others being completely discharged. The consequences of this imbalance are over-voltage, capacitor damage, and drastically reduced lifetime. [18]

2.4.1.3 Polypropylene Film Capacitors

Film capacitors are composed of metal foil, used as an electrode, and plastic films overlapped from both ends wounding into a cylindrical structure. The dielectric of such capacitors is made up of a film of polypropylene. The capacitor core is packed in plastic with a metal casing. Such capacitors have a wide range of applications such as daily household appliances, laser, filtering, etc.

Unlike electrolytic capacitors, film capacitors show constant capacitance over a wide range of frequencies specifically from 100 Hz to 200 kHz. In addition to that, the ESR of these capacitors also remains unchanged in the said frequency range. Another differing factor is the effect of temperature fluctuations on the capacitance and ESR. Film capacitors show significantly fewer deviations in ESR and capacitance caused by temperature fluctuations. [17], [19]
Tab. 2.1 enlists a summarized comparison of the above types of capacitors. [17]

Tab. 2.1: Comparison of Types of DC link capacitors

	Aluminium Electrolytic Capacitors	Film Capacitor
Common mode failure	parametric failure, open circuit	parametric failure, open circuit
Common failure cause	Electrolyte loss	Loss of dielectric area
Important Stressors	$\vartheta_{\text{ambient}}$, I_{ripple}, $V_{\text{operating}}$	$\vartheta_{\text{ambient}}$, $V_{\text{operating}}$, humidity
self healing	yes	yes

2.4.1.4 Ceramic Chip Capacitors

Ceramic chip capacitors have a ceramic layer/layers serving as dielectric. In practice, these are often composed of multiple ceramiclayers and hence are known as Multi Layer Ceramic Capacitors (MLCCs). The multiple layering provides more capacitance while retaining a small size. In addition to that, ceramic capacitors have a low equivalent ESR which in turn translates into low discharging and charging times. Such capacitors are ideal for applications where space is limited. Such an example would be small or compact PCBs with a dense design (e.g. mobile devices, power supplies, filters, etc). [20]

In addition to the above, such capacitors are also susceptible to changes in capacitance on the application of DC voltage. This is due to the nonlinear behavior of dielectric material present in the capacitors. The dielectric constant of such material also varies along applied voltage, temperature, and frequency. This happens because in DC biasing, the alignment of dipole moments within the dielectric material gets affected, due to which the material's ability to store electric charge changes. As the DC voltage increases, the effective dielectric constant decreases, reducing the capacitor's capacitance. [21]

2.4.2 Silicon Carbide Power Switches

Many SiC power MOSFETs are available on the market. To find the best-suited one for this drive inverter application, a first comparison between discrete SiC devices and SiC power modules is done before the methodology for the power loss analyses is presented.

2.4.2.1 Discrete SiC Devices

Discrete SiC devices or components are silicon carbide-based semiconductor devices. Such devices have various characteristics such as greater power density, high efficiency, and the ability to operate at high temperatures and voltages. The following components are included when referring to discrete SiC devices:

- SiC MOSFETs
- SiC JFETs
- SiC IGBTs
- SiC BJTs
- SiC Gate Turn-Off Thyristors
- SiC Schottky Diodes

Discrete SiC devices have many applications such as renewable energy systems (solar and wind power inverters), Electric Vehicles (EVs) and Hybrid Electric Vehicles (HEVs) for both traction and charging, power supplies for data centers, industrial motor drives, and High Voltage Direct Current (HVDC) transmission systems. Their selection criteria are based on the need for more efficient, compact, and reliable power electronic systems capable of operating under various conditions.

2.4.2.2 SiC Power Modules

SiC power modules are modules that are based on SiC semiconductors. These are generally used for higher electrical efficiency in power transformation. SiC power modules have a variety of applications which are as follows:

- Solar inverters
- Uninterruptible power supplies
- Power supplies
- Motor drives

2.4.2.3 Electrical Characteristics in terms of Parasitic Effects

The compact and integrated design of SiC power modules allows them to exhibit lower parasitic inductance and parasitic capacitance. This is due to the minimized current path length between the devices. The lower parasitic inductance is beneficial and important for

high-frequency operation for reducing switching losses. It thus improves the efficiency and performance of the system as a whole along with less overshoot voltage during switching, enhancing the module's reliability. SiC power modules' better parasitic capacitance allows efficient switching. [22]

2.4.2.4 Power Loss Analyses Methodology

As the modules outperform the discrete devices in terms of parasitic elements and power density, only modules will be compared by power loss analyses and used for the inverter design. During the analyses, a stationary operating point is considered, as a non-stationary analysis requires a complete simulation model for the modules. Also, a Sine Triangular Modulation is assumed for simplification reasons, as the exact modulation scheme needs to be developed in a further project. Additionally, current ripple and other deviations from a pure sine wave, which are a result of the switching behavior, are also neglected.
The estimations are based on the drain-source on resistance $R_{\mathrm{DS,on}}$ and the on and off switching losses, E_{on} respectively E_{off}, according to the applied drain current i_{D} of the individual modules, taken from their datasheets. As the parameters vary with the junction temperature, a stationary operating temperature of 125 °C is assumed. Most modules are also specified for temperatures of around 150 °C or even at 175 °C, but the switches will not be operated at these hot temperatures by the UPBracing Team to ensure, that the modules will not be damaged due to over temperature. Thus, a junction temperature of 125 °C is assumed, which is quite high but has a reasonable safety margin to the absolute maximum temperature, and damage due to over temperature is therefore rather unlikely.
The first and fastest estimation method is to calculate the average power losses during one period of the sinusoidal drain current with an assumed DC drain current $I_{\mathrm{D,RMS}}$, which is the Root Mean Square (RMS) equivalent current of the normally applied AC drain current. The conduction losses can be calculated to be

$$P_{\mathrm{cond}}(I_{\mathrm{D,RMS}}) = R_{\mathrm{DS,on}} \cdot \frac{1}{T_{\mathrm{sine}}} \cdot \int_0^{T_{\mathrm{sine}}} i_{\mathrm{D}}^2 \mathrm{d}t \tag{2.3}$$

$$= R_{\mathrm{DS,on}} \cdot \sqrt{\frac{1}{T_{\mathrm{sine}}} \cdot \int_0^{T_{\mathrm{sine}}} i_{\mathrm{D}}^2 \mathrm{d}t}^2 \tag{2.4}$$

$$= R_{\mathrm{DS,on}} \cdot I_{\mathrm{D,RMS}}^2 \tag{2.5}$$

and for the switching losses results

$$P_{\mathrm{sw}}(I_{\mathrm{D,RMS}}) = 2 \cdot f_{\mathrm{sw}} \cdot (E_{\mathrm{on}}(I_{\mathrm{D,RMS}}) + E_{\mathrm{off}}(I_{\mathrm{D,RMS}})) \tag{2.6}$$

where f_{sw} stands for the frequency of the triangular carrier. The factor 2 needs to be considered here, since there are two switching events during one period of the triangular carrier T_{sw}. This can be seen in Fig. 2.7, here the carrier u_{Δ} has a period of 0.1 ms and the switching events are represented by rising and falling edges of s_{U}. During one carrier period, there are always one rising and one falling edge, thus two switching events.

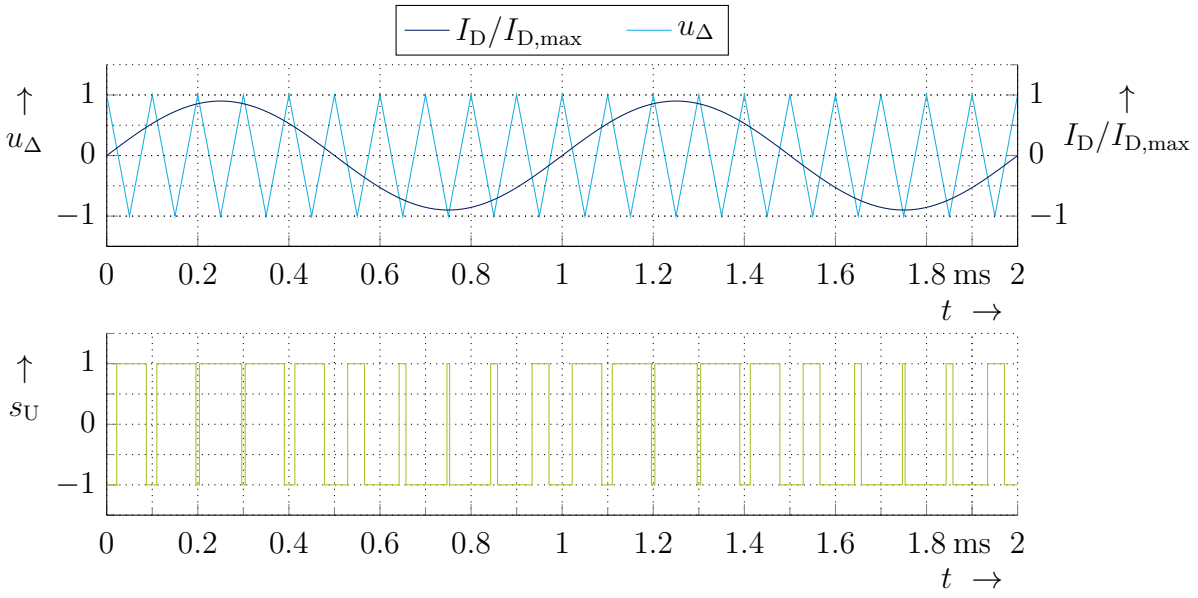


Fig. 2.7: Sine triangular modulation

The issue hereby is that the switching losses do not scale with the square of the drain current. This means, that the switching losses calculated with Eq. 2.6 for the RMS equivalent current $I_{D,RMS}$ do not represent the exact mean switching power losses of the AC drain current during one period T_{sine}.
A more precise power loss estimation can be done by sampling the sinusoidal drain current every $\Delta T_j = j \cdot T_{sw}$ and summing up the corresponding switching energy losses for one sinusoidal drain current period. After dividing the integrated switching energy losses by the integration period of the sinusoidal drain current, the result is a more realistic estimation of the switching power losses:

$$P_{sw} = \frac{1}{T_{sine}} \cdot \sum_{j=0}^{\frac{T_{sine}}{T_{sw}}} \int_0^{T_{sine}} \delta\left(t - \Delta T_j\right) \cdot \left(E_{on}\left(\delta\left(t - \Delta T_j\right) \cdot i_D\left(t\right)\right) + E_{off}\left(\delta\left(t - \Delta T_j\right) \cdot i_D\left(t\right)\right)\right) \mathrm{d}t \tag{2.7}$$

$$= \frac{1}{T_{sine}} \cdot \sum_{j=0}^{\frac{T_{sine}}{T_{sw}}} \left(E_{on}\left(\delta\left(t - \Delta T_j\right) \cdot i_D\left(t\right)\right) + E_{off}\left(\delta\left(t - \Delta T_j\right) \cdot i_D\left(t\right)\right)\right) \tag{2.8}$$

$$= \frac{1}{T_{sine}} \cdot \sum_{j=0}^{\frac{T_{sine}}{T_{sw}}} \left(E_{on}\left(i_D\left(j \cdot T_{sw}\right)\right) + E_{off}\left(i_D\left(j \cdot T_{sw}\right)\right)\right) \tag{2.9}$$

3 Drive Inverter Development

3.1 Overall Requirements

The development of a drive inverter for a Formula Student race car of the UPBracing Team is bound on the one hand by the Formula Student regulations and the requirements of the UPBracing Team. On the other hand, the drive inverter should fit into the existing vehicle ecosystem with its interfaces for interaction with the race car.

3.1.1 Formula Student Regulations

During the development of the drive inverter, especially the galvanically isolation between TS and LVS needs to be considered. This means, at least a spacing of 4 mm between TS and LVS must be ensured, if conformal coating is used. A detailed overview of permitted spacing distances is given in section 2.1.4. Isolation barrier components need to be selected according to their isolation voltage rating in the datasheets (see section 2.1.3). The maximum TS voltage is already limited by the TS Battery Management System and does not need to be monitored by the drive inverter additionally. Regarding possible soldered connections in the high current path, which mainly includes the TS input and phase output terminals, the power switches, and the current sensing circuit, each of these individual components must be secured through an additional fastening besides the solder points in the high current path or must be connected to the PCB through another mechanism than soldering (see section 2.1.5). The inverter must also indicate, if the voltage across the DC link capacitance is over 60 V. The voltage detection circuit must be fully designed in hardware (see section 2.1.9).

3.1.2 Requirements of the UPBracing Team

As the UPBracing Team does not have unlimited financial resources, the drive inverter should be cost effective. If possible, the components used should therefore be selected from one of the sponsors of the UPBracing Team, namely Würth Elektronik, STMicroelectronics, Infineon, and LEM. Additionally, a functional separation into different PCBs is strived for. This can reduce the manufacturing costs of the PCBs, as the individual boards can be customised according to the functional groups in terms of layer thickness, number of layers

and size. Furthermore, the packaging of several PCBs can be more compact than a big one. Especially, it is to be assumed that a new inverter design cannot be developed each year again, so separation into several PCBs might be an advantage to adapt the inverter systems packaging to the available space of each vehicle. A last benefit of splitting the system into several PCBs is the simplified maintenance. In case of a failure, only one smaller PCB needs to be exchanged instead of the whole drive inverter design.
To minimize the weight of every race car is one top goal as the weight has a direct impact on the performance. Therefore, the inverter design should be smaller in volume and more lightweight than the existing, purchased inverter, which has a volume of about $14\,\mathrm{cm} \cdot 19\,\mathrm{cm} \cdot 10\,\mathrm{cm} = 2660\,\mathrm{cm}^3$ and weights 1200 g. The inverter's switching frequency has also a direct impact on the necessary minimum DC link capacitance (see Eq. 2.1). Therefore a switching frequency of $f_{\mathrm{sw}} = 20\,\mathrm{kHz}$ is targeted to decrease the necessary minimum volume captured by the DC link, to smooth the phase current and thus minimize the torque ripple of the motor. Because the power losses increase with the switching frequency, the losses of the complete inverter should not exceed 400 W due to the high switching frequency, as the inverter would then be more inefficient as the purchased Insulated Gate Bipolar Transistor (IGBT) inverter with a switching frequency of 8 kHz and a phase current of $61\,\mathrm{A_{RMS}}$. Additionally, the inverter should be designed in a way, that it can be operated with a coldplate temperature up to at least 70 °C, as the outside temperatures during a race in the sun can reach beyond 35 °C and cooling liquid temperatures up to 60 °C are not unusual.
The UPBracing Team's long-term plan is to develop optimized electrical motors in addition to an inhouse developed drive inverter. However, it is currently not certain whether such a motor can be installed in the car at the same time as the inverter. Thus, it should be paid attention to developing an inverter which is compatible with the motors used so far but is more optimized for the new motors that should be used soon. So, on the one side, the inverter should be able to provide a phase current of up to $72.83\,\mathrm{A_{RMS}}$ which is the maximum current of the motors used so far but be more efficient with the new motors, which have a maximum current of $61\,\mathrm{A_{RMS}}$. Additionally, the motor encoder interface should also be compatible with both motors.
To estimate the necessary minimum capacitance according to Eq. 2.1, a maximum power variation of two times the nominal motor power can be assumed, as this will occur during start-up with operation at the current limit of the motor [14]. The necessary output power of the isolated gate driver power supplies can be calculated according to [23] as the product of the gate charge $Q_{\mathrm{G}} = 0.3\,\mu\mathrm{C}$, the maximum voltage swing $\Delta V_{\mathrm{GS}} = 20\,\mathrm{V}$ and the switching frequency of $f_{\mathrm{sw}} = 20\,\mathrm{kHz}$

$$P_{\mathrm{G}} = Q_{\mathrm{G}} \cdot \Delta V_{\mathrm{GS}} \cdot f_{\mathrm{sw}} \tag{3.1}$$
$$= 0.3\,\mu\mathrm{C} \cdot 20\,\mathrm{V} \cdot 20\,\mathrm{kHz} \tag{3.2}$$
$$= 0.12\,\mathrm{W} \tag{3.3}$$

It is recommended by [23] to add extra 0.3 W for gate driver internal power dissipation, so that a gate power of $P_{\mathrm{G}} = 0.42\,\mathrm{W}$ results. To ensure a proper operation and to have some safety margin, a isolated gate driver power supply with at least 1 W is necessary.

3.1.3 Drive Inverter Interfaces and Interaction with the Race Car

Communication in the race car is based on CAN. The existing car interface for the drive inverter therefore has a CAN port besides a 24 V supply input. To allow the inverter to influence the SDC, corresponding input and output ports are also provided. To ensure, that the motors are only activated when the SDC is completely closed and the output stage should be released, an extra SDC enable signal is connected to the inverter, which in principle is the end of the SDC after the last switch which can open the SDC.
For proper functionality of the TSAL, an output signal for the over 60 V detection of the DC link capacitance is established, together with a separate signal ground port. At the high voltage side, the TS power input is directly connected with the TS battery. The three motor phases are connected to the corresponding motor windings. For motor temperature and position monitoring a motor encoder connection is established. The temperature is transmitted via an analog signal since the temperature sensor is either a KTY in the old motors or a PT1000 in the new motors. The communication with the motor encoder for position monitoring of the rotor is based on an EnDat 2.2 interface. Therefore, six extra ports need to be provided for the supply voltage of the encoder, the two clocks and the two data lines. Fig. 3.1 visualizes the inverter interface in a block diagram.

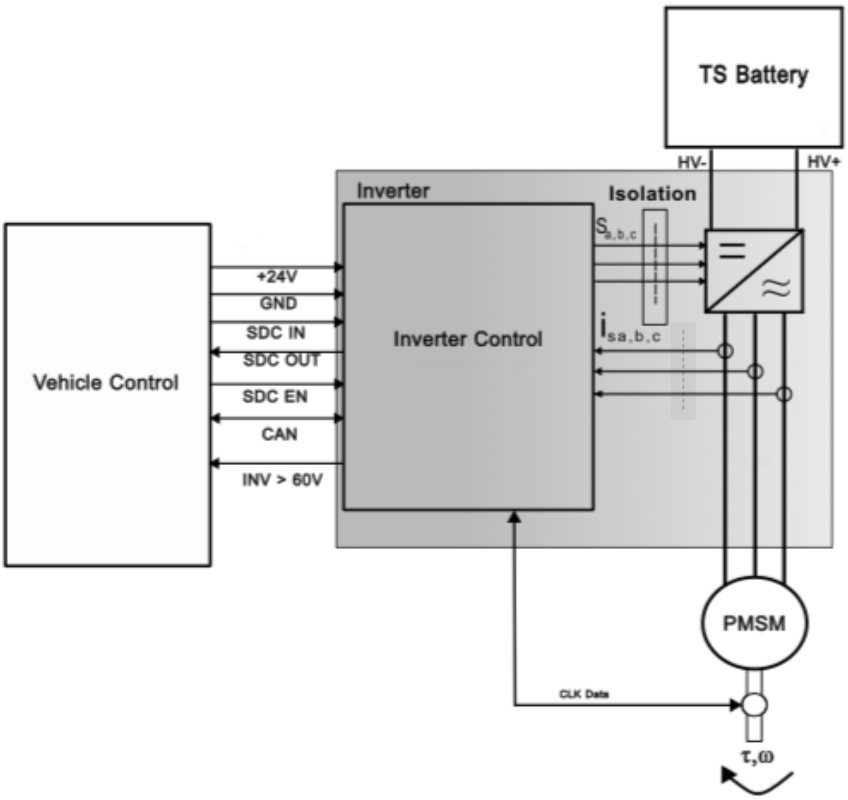


Fig. 3.1: General Block diagram of the inverter system

3.2 Selected Components

To select proper components, the considerations and equations from chapter 2 are taken into account. As a first estimation of the necessary DC-link capacitance, Eq. 2.1 is used for a DC link voltage of $V_{\mathrm{DC}} = 600\,\mathrm{V}$, a maximum power variation of two times the nominal power $\Delta P_{\mathrm{max}} = 2 \cdot 16\,\mathrm{kW} = 32\,\mathrm{kW}$, a switching period of $T_{\mathrm{sw}} = \frac{1}{f_{\mathrm{sw}}} = \frac{1}{20\,\mathrm{kHz}} = 50\,\mu\mathrm{s}$ and a maximum voltage fluctuation of $\Delta V_{\mathrm{DC}} = 10\,\% \cdot V_{\mathrm{DC}} = 60\,\mathrm{V}$:

$$C_{\mathrm{DC,min}} \geq \frac{\Delta P_{\mathrm{max}} \cdot T_{\mathrm{sw}}}{2 \cdot V_{\mathrm{DC}} \cdot \Delta V_{\mathrm{DC}}} \tag{3.4}$$

$$= \frac{2 \cdot 16\,\mathrm{kW} \cdot 50\,\mu\mathrm{s}}{2 \cdot 600\,\mathrm{V} \cdot 60\,\mathrm{V}} \tag{3.5}$$

$$= 22\,\mu\mathrm{F} \tag{3.6}$$

As a second step, the expected current ripple according to Eq. 2.2 is estimated as a function of the Modulation Index M and the Power Factor $\cos(\varphi)$.

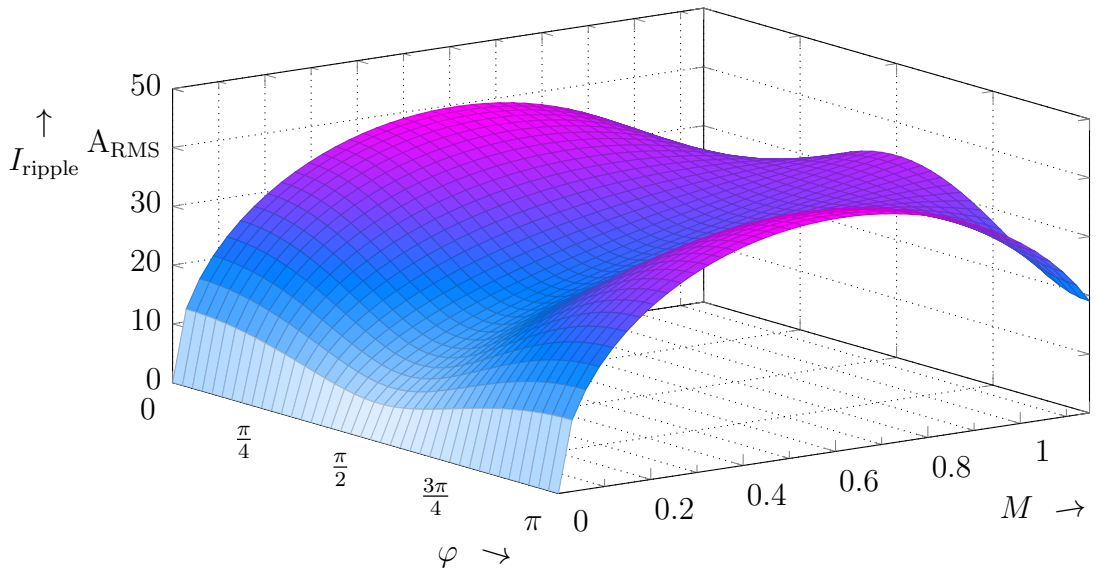


Fig. 3.2: Current ripple I_{ripple} as a function of the Modulation Index M and the phase shift angle φ

Fig. 3.2 shows the relation between Modulation Index M, phase shift angle φ and the expected current ripple I_{ripple} for a maximum phase current of $\hat{I}_{\mathrm{max}} = 86.27\,\mathrm{A}$, which is the peak value for a RMS drain current of $61\,\mathrm{A_{RMS}}$. It can be recognised, that a maximum current ripple of $I_{\mathrm{ripple,max}} = 39\,\mathrm{A_{RMS}}$ occurs at $M = 0.61$ and every $\varphi = n \cdot \pi$ with $n \in \mathbb{N}_0$. But these operating points will never occur, because a phase shift angle of $\varphi = 0$ can only appear in totally resistive systems, since voltage and current must be in phase for this, and a PMSM has an inductive component because of the windings. Additionally, the

maximum phase shift angle of totally inductive respectively capacitive systems is $|\varphi| = \frac{\pi}{2}$. However, to ensure that the capacitors are not damaged due to overload or stresses near their limits, the DC link should have a total current ripple capability of at least $40\,\mathrm{A_{RMS}}$, since the real current ripple may also vary.

Due to the maximum TS voltage of 600 V and the limited voltage rating of electrolytic capacitors up to 650 V, these capacitor types are not very suited for this inverter design, as there is only a safety margin of around 50 V and a balancing circuit required for the series connection of multiple capacitors complicates the whole design. Ceramic chip capacitors achieve high capacitance in a small size, but the DC bias effect makes the behavior in the real application difficult to predict because of the decrease in capacitance with increasing voltage. Therefore, film capacitors are chosen for this inverter design, as they offer constant capacitance over a wide frequency range and have less deviations in ESR and capacitance due to temperature changes.

With the above restrictions, the best-suited DC link film capacitor from the UPBracing Team's sponsor Würth Elektronik is selected. For this, the capacitance to volume efficiency and the current ripple capability to volume efficiency are calculated for every DC link capacitor with a voltage rating of more than 800 V. Additionally, the total quantity of capacitors N_C to achieve the requirements is also calculated. It can be noticed that, with two exceptions, generally more capacitors need to be connected in parallel to achieve the required current ripple capability of $40\,\mathrm{A_{RMS}}$ than the total capacitance of 22 µF. The chosen capacitor has the best balance between the total occupied volume V_total and the total capacitance $C_\mathrm{total} = N_\mathrm{C} \cdot C_\mathrm{single}$ while complying with the required current ripple capability.

Tab. 3.1: Comparison of DC link capacitors (C_single and $I_\mathrm{ripple,single}$ taken from [24])

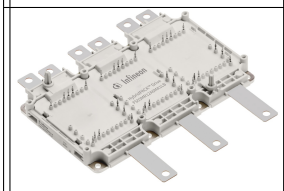
MPN	C_single in µF	$I_\mathrm{ripple,single}$ in $\mathrm{A_{RMS}}$	N_C for $I_\mathrm{ripple} = 40\,\mathrm{A_{RMS}}$	V_total in $\mathrm{cm^3}$	C_total in µF
890724427010CS	10	12.2	4	104.192	40
890494427003CS	3	5.2	8	94.080	24
890734427005CS	3	6.5	7	107.520	21
890744427001CS	1	3.5	12	84.480	12
890744427005CS	5	10.4	4	104.192	20

Tab. 3.1 shows all DC link capacitors, that have a total volume of less than $110\,\mathrm{cm^3}$ and also achieve a current ripple capability of at least $40\,\mathrm{A_{RMS}}$. It can be seen that the 890724427010CS has in total the best ratio between total volume and total capacitance and will therefore be used for this drive inverter design. The other capacitors either do not achieve a total capacitance of 22 µF or have only slightly more than the required capacitance but with a disproportionately high total volume.

To decide for the best suited SiC MOSFET module, a first selection is done according to the datasheets of different modules. Here the continuous DC drain current should be

higher than 61 A to ensure a reliable operation of the motors even during continuous high load and to protect the modules from overheating. Additionally, the internal configuration of the MOSFETs should be either already a complete inverter bridge or a half-bridge, in order to combine three half-bridge modules into one inverter bridge.

Tab. 3.2: SiC MOSFET module housings from Infineon (pictures and values taken from [25])

Picture	Housing	Weight in g	Length in mm	Width in mm	Height in mm
 Typical appearance	Easy 1B	24	63	34	12
	Easy 2B	39	63	57	12
 Typical appearance	Easy 3B	78	110	62	12
 Typical appearance	62 mm	340	106	61	31
	HybridPack Drive	720	155	127	32

As a third selection criteria, the weight and size of the modules is taken into account. Generally, the Easy 1B and Easy 2B housings from Infineon have a weight of 24 g respectively 39 g, which are quite close to each other compared to bigger housings like the

62 mm housing (340 g) or the HybridPack Drive housing (720 g). The Easy 3B housing is also rather lightweight with 78 g but significantly bigger than the Easy 1B or Easy 2B housings like it can also be seen in Tab. 3.2. Therefore, only modules in a Easy 1B or Easy 2B housing are compared by power loss analyses, as these modules are the smallest and most lightweight ones, and thus best suited for this design. Furthermore, the bigger modules are also more designed to handle higher currents of up to 560 A continuously. Therefore they have a lower drain source on resistance, but also increased switching losses that will dominate the total losses at higher switching frequencies and thus lead to a decrease in efficiency. This can even be seen for the Easy 1B modules in the power loss analysis below.

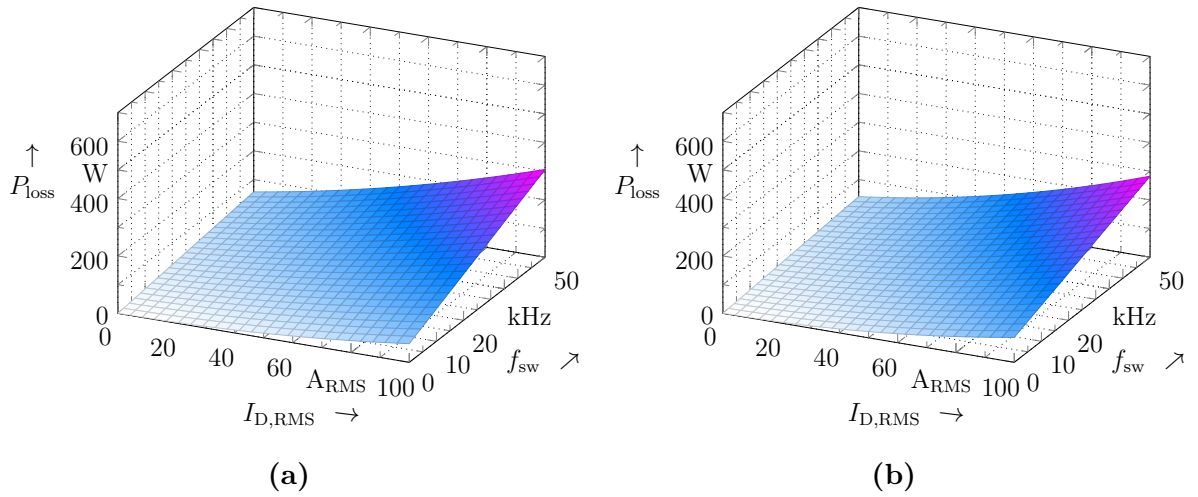
Tab. 3.3: SiC MOSFET modules from Infineon (values taken from [25])

MPN	Housing	$R_{DS,on}$ in mΩ		E_{on} in mJ		E_{off} in mJ	
		25 °C	125 °C	25 °C	125 °C	25 °C	125 °C
FF4MR12W2M1H_B70 FF4MR12W2M1HP_B11 FF4MR12W2M1H_B11	Easy 2B	4	6.5	3.22	3.77	0.84	0.85
FF6MR12W2M1HP_B11 FF6MR12W2M1H_B11 FF6MR12W2M1H_B70	Easy 2B	5.4	8.7	1.69	2.14	0.98	0.99
FF08MR12W1MA1_B11A	Easy 1B	7.33	10.6	4.26	5.01	2.67	2.73
FF8MR12W1M1H_B11 FF8MR12W1M1H_B70	Easy 1B	8.1	13.1	2.87	3.05	0.75	0.81
FF11MR12W2M1HP_B11	Easy 2B	10.8	17.4	1.38	1.68	0.38	0.42
FF11MR12W2M1H_B70	Easy 2B	10.8	17.4	1.12	1.39	0.53	0.6
FS13MR12W2M1HP_B11 FS13MR12W2M1H_C55 FS13MR12W2M1H_B70	Easy 2B	11.7	18.9	1.39	1.57	1.06	1.14

Tab. 3.3 compares all modules that were filtered out using the above criteria. The power loss analysis regarding chapter 2.4.2 is done. As a first estimation, only the RMS equivalent DC drain current is assumed. The losses are calculated for a RMS drain current range of $I_{\mathrm{D,RMS,min}} = 0\,\mathrm{A_{RMS}}$ to $I_{\mathrm{D,RMS,max}} = 100\,\mathrm{A_{RMS}}$.
The conduction losses are calculated according to Eq. 2.5 while the drain-source on resistances $R_{\mathrm{DS,on}}$ can be considered as a shape parameter for the different modules.
To estimate the switching losses, Eq. 2.6 is taken into account, here E_{on} and E_{off} also serves as a shape parameter for the different modules. The switching frequency f_{sw} is also swept from $f_{\mathrm{sw,min}} = 0\,\mathrm{Hz}$ to $f_{\mathrm{sw,max}} = 50\,\mathrm{kHz}$, so that the switching losses can be calculated as a function of the switching frequency.

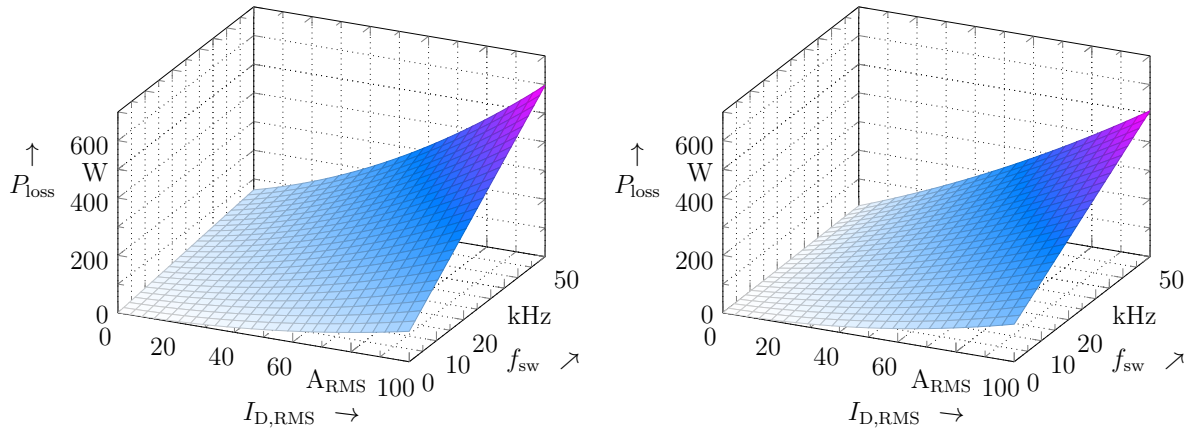
Fig. 3.3 to 3.6 visualize the total power losses of the different modules for one complete half bridge (two transistors) as a function of the RMS drain current $I_{\mathrm{D,RMS}}$ and the switching frequency f_{sw}. To get a first impression of the modules' efficiencies at maximum load,

the power losses at maximum drain current $I_{\mathrm{D,RMS,max}} = 100\,\mathrm{A}$ and maximum switching frequency $f_{\mathrm{sw,max}} = 50\,\mathrm{kHz}$ can be compared.



(a) **(b)**

Fig. 3.3: Total power losses of module family (a) FF4MR12W2M1H and (b) FF6MR12W2M1H



(a) **(b)**

Fig. 3.4: Total power losses of module (a) FF08MR12W1MA1_B11A and module family (b) FF8MR12W1M1H

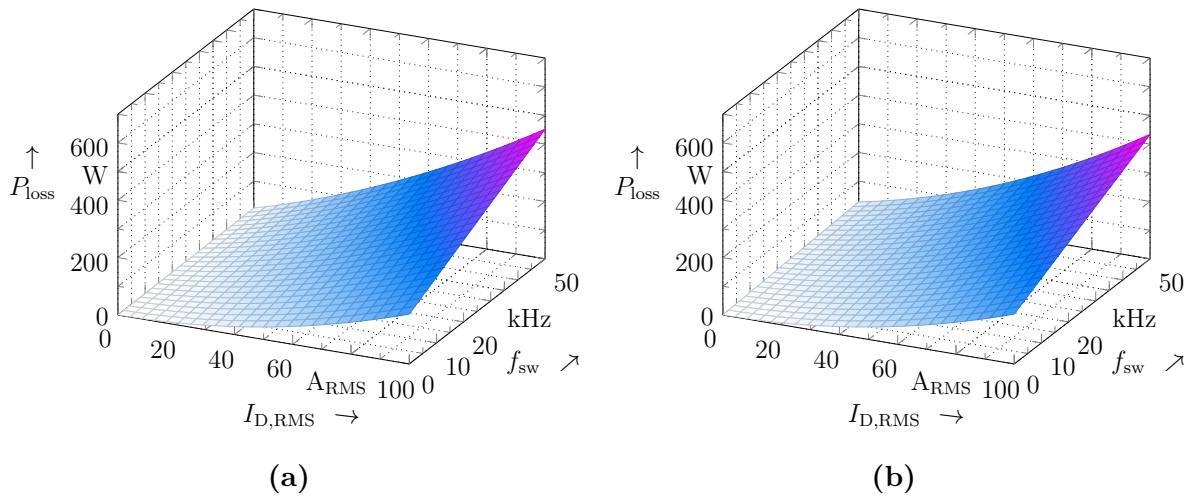


Fig. 3.5: Total power losses of modules (a) FF11MR12W2M1HP_B11 and (b) FF11MR12W2M1H_B70

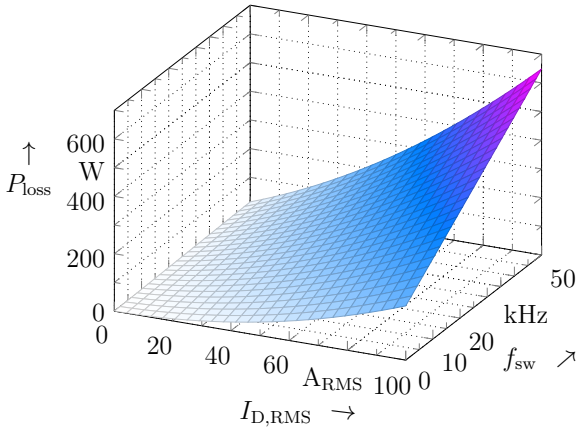


Fig. 3.6: Total power losses of module family FS13MR12W2M1H

In summary, it can be stated that the module families FF4MR12W2M1H and FF6MR12W2M1H seems to have the best peak performance with around 300 W. The modules FF11MR12W2M1HP_B11 and FF11MR12W2M1H_B70 dissipate 100 W more power and thus have a mediocre efficiency. The highest power dissipation under peak load conditions seems to occur with the module families FF8MR12W1M1H (500 W), FS13MR12W2M1H (650 W) and with module FF08MR12W1MA1_B11A (600 W).

However, the modules will not be operated at these limits, especially not at a switching frequency of $f_{sw,max} = 50\,kHz$. Therefore, Fig. 3.7 compares the modules at the switching frequency $f_{sw} = 20\,kHz$, which is targeted by the UPBracing Team. At 20 kHz it can be noticed, that for lower currents up to 30 A, the power losses of the modules are very

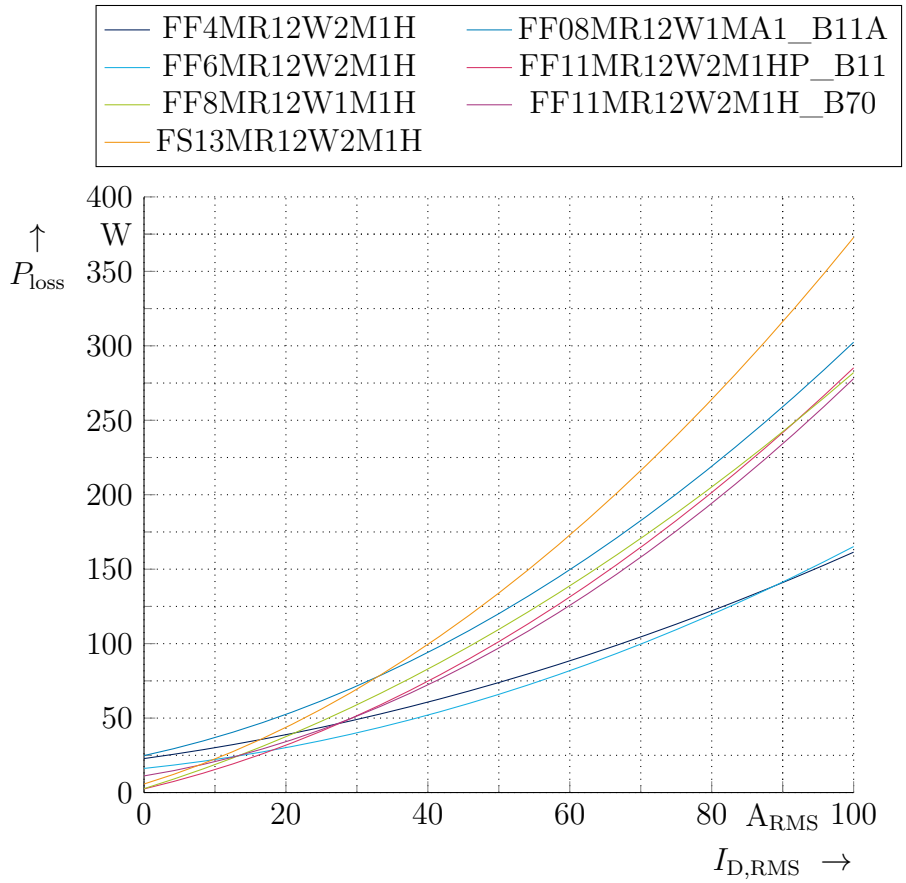


Fig. 3.7: Total average module power losses at $f_{\text{sw}} = 20\,\text{kHz}$ calculated with the RMS current method

similar, since the losses only vary by 30 W. Especially modules with a higher drain source on resistance and therefore lower switching losses operate in a more efficient way at lower currents, e.g. the FS13MR12W2M1H or FF8MR12W1M1H module families. At higher currents, these modules have a worse efficiency than modules with a lower drain source on resistance, but higher switching losses, like the FF11MR12W2M1H_B70. Two module families have a conspicuous efficiency, the FF4MR12W2M1H and the FF6MR12W2M1H have significantly lower losses at higher currents than the other modules.

However, as already mentioned in section 2.4.2, the RMS current power loss analysis may not estimate the real module power losses due to the neglect of current dependent switching losses. Therefore, a second power loss analysis is done, which is based on the Sine Triangular Modulation. Fig. 3.8 (top) depicts the triangular carrier with a switching frequency of 20 kHz and the targeted sinusoidal current with an amplitude of 61 A_{RMS} and a frequency of 500 Hz in a steady state. The estimated energy losses during the switching events are depicted in the bottom diagram of Fig. 3.8. The modules' average power losses during one current period can then be calculated as the sum of the average

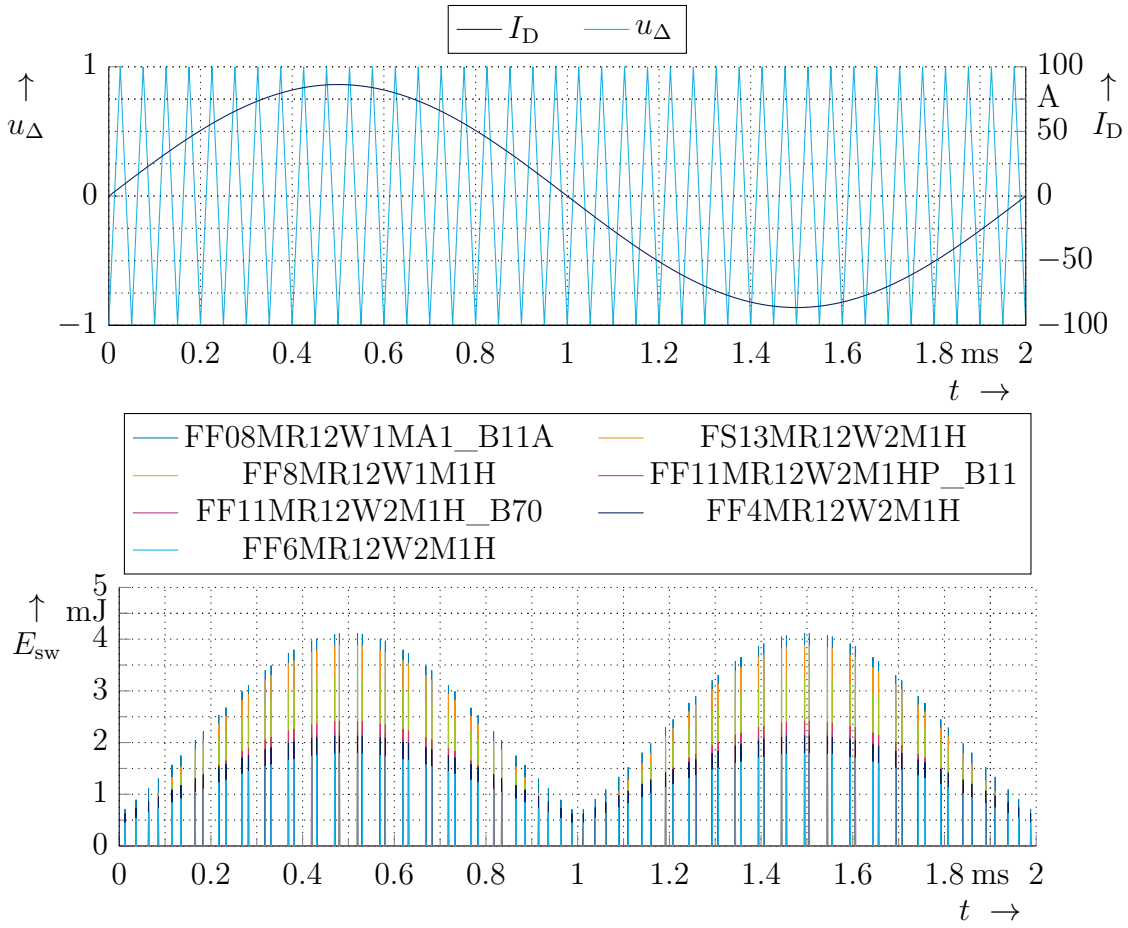


Fig. 3.8: Sine Triangular Modulation (top) and deviated modules switching losses at switching events (bottom)

conduction losses (refer to Eq. 2.5) and the average switching losses (refer to Eq. 2.9). The average total power losses of the modules during one current period estimated with the Sine Triangular Modulation are visualized in Fig. 3.9. Compared with Fig. 3.7, it can be seen, that there are no big differences between the calculated power losses with the RMS current method and the Sine Triangular Modulation method. The losses calculated with the Modulation are only around 4 % lower than of the RMS current method. This is a big advantage of the RMS current method, since it calculates the losses much faster and with less computation effort, when the focus is on a first rough estimation of the losses. For more precise estimations, a complete module simulation model is necessary.

To support this theses, the modules are also compared in Infineon's online simulation tool IPOSIM. It is assumed, that IPOSIM estimates the power losses in a more precise way, since it is provided by the manufacturer of the modules, who has the most knowledge of their behavior and their power losses. Fig. 3.10 shows the simulation results. The simulations are done with the same parameters for the current and the switching frequency

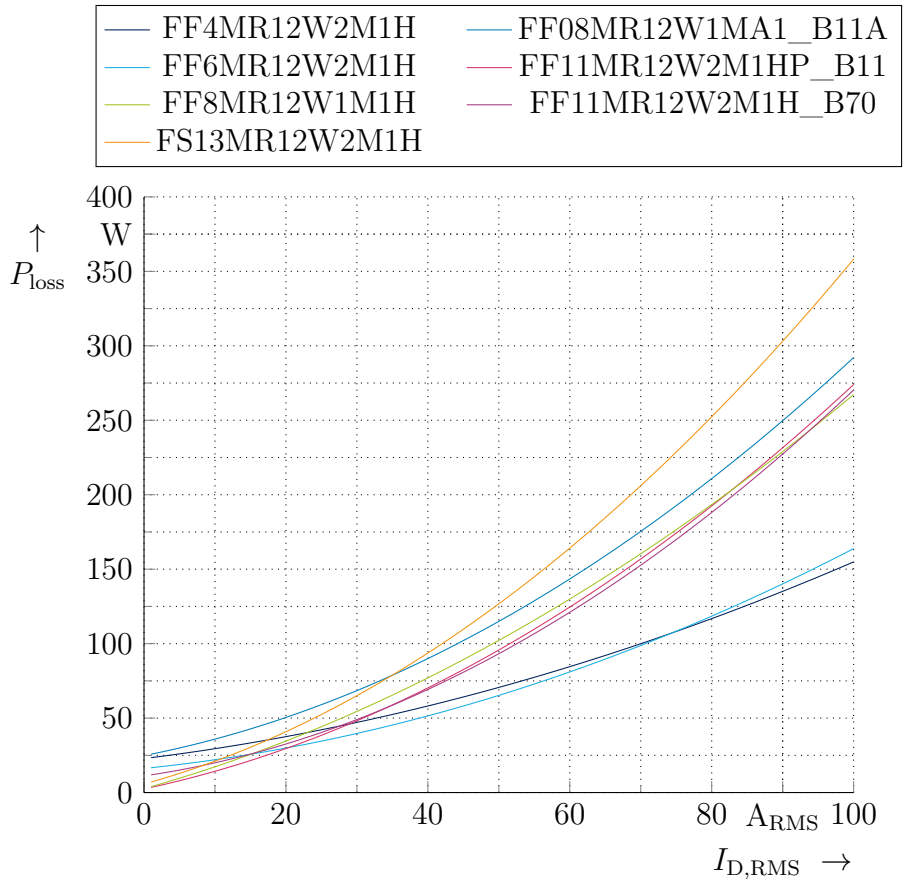


Fig. 3.9: Total average module power losses at $f_{\text{sw}} = 20\,\text{kHz}$ calculated with the Modulation method

as the above power loss calculations. It can be noticed that the power losses simulated with IPOSIM are significantly lower than with the other two calculation methods, e.g. for the module family FS13MR12W2M1H it is a decrease of around 75 A at $I_{\text{D,RMS}} = 100\,\text{A}_{\text{RMS}}$. Furthermore, especially at low drain currents of up to $I_{\text{D,RMS}} = 20\,\text{A}_{\text{RMS}}$ the module losses are more similar and tend to $P_{\text{loss}}(0\,\text{A}_{\text{RMS}}) = 0\,\text{W}$ with decreasing drain current. With the assumption that IPOSIM simulates the most realistic power losses due to Infineon's unique knowledge of its modules, it can be stated, that the other two calculation methods overestimate the module losses by a factor of around 25 % to 30 %, which is quite high. But the development of the losses with increasing drain current still seems to be realistic.

As a summary of the power loss estimation methods, it can be said, that the RMS method delivers the fastest results with a very manageable computation effort. However, a overestimation of up to 30 % must be expected. But it is especially useful to get a first assessment of the expected losses and the relationship between losses and drain current and also to roughly compare different modules. The Sine Triangular Modulation method needs more effort and time to calculate the losses. The results are losses that are around

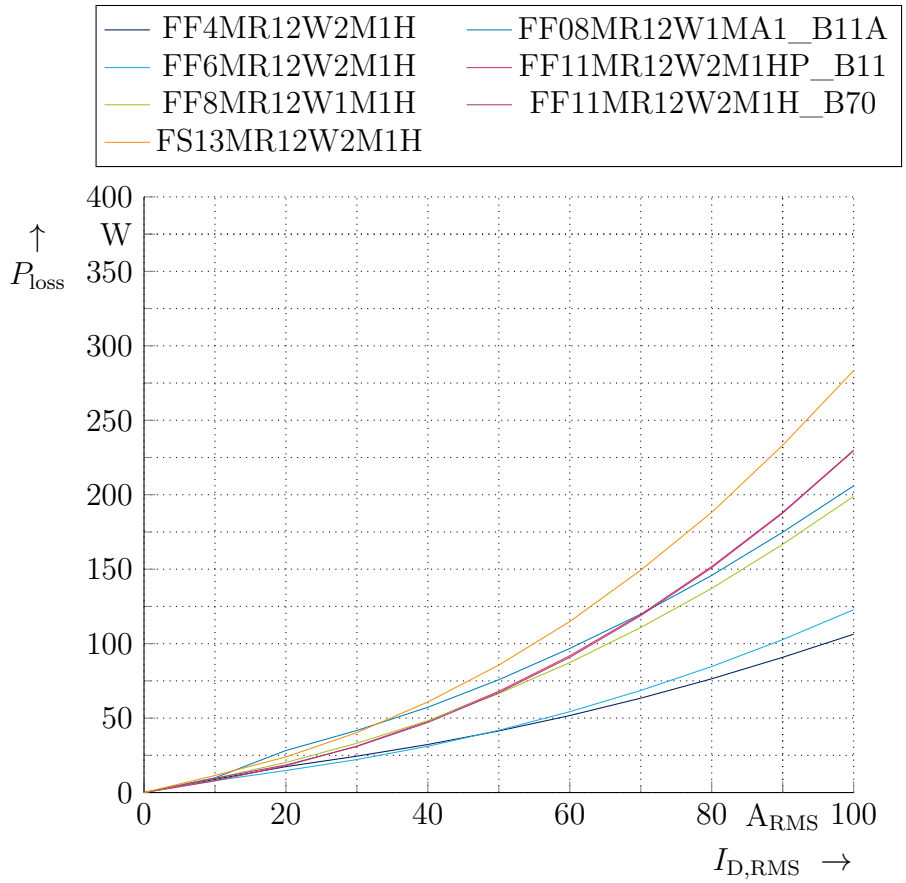


Fig. 3.10: Total average module power losses at $f_{\text{sw}} = 20\,\text{kHz}$ simulated with IPOSIM

2 % less overestimated. Therefore, this modulation method has a worse cost-benefit ratio, when assuming the IPOSIM results to be realistic. However, to make more meaningful statements, the estimation methods need to be validated by laboratory power loss analyses of the individual modules.

Before finally deciding for a module, it can be said first, that most modules seem to be able to handle drain currents of up to $I_{\text{D,RMS,max}} = 100\,\text{A}_{\text{RMS}}$ with a realistic necessary coldplate temperature, which was also taken into account for the simulations in IPOSIM. Only the module family FS13MR12W2M1H needs quite low coldplate temperatures of 31 °C in order to keep the junction temperature around 125 °C at $I_{\text{D,RMS,max}} = 100\,\text{A}_{\text{RMS}}$. However, this coldplate temperature does not comply with the requirement of the UPBracing Team. The necessary coldplate temperatures of the other modules are all higher than 70 °C. Thus, the smallest and lightweight module is chosen, which also has the best ratio of efficiency to necessary coldplate temperature. As the module families FF4MR12W2M1H, FF6MR12W2M1H and the modules FF11MR12W2M1HP_B11 and FF11MR12W2M1H_B70 have a Easy 2B housing, which is larger than the Easy 1B housing in which the other remaining modules are installed, they are sorted out. The best suited module for this drive inverter therefore has

to be chosen from the module family FF8MR12W1M1H, as the FF08MR12W1MA1_B11A has higher losses. The modules of the FF8MR12W1M1H family are specified with equal drain source on resistance and switching energy losses as can be seen in 3.3. But, according to their datasheets, the module FF8MR12W1M1H_B70 has a lower thermal resistance with $R_{\mathrm{TH,JH,B70}} = 0.311\,\frac{\mathrm{K}}{\mathrm{W}}$ than the FF8MR12W1M1H_B11 ($R_{\mathrm{TH,JH,B11}} = 0.553\,\frac{\mathrm{K}}{\mathrm{W}}$). Due to the lower thermal resistance, the maximum allowed coldplate temperature can be further increased. However, the FF8MR12W1M1H_B70 is also more expensive. Thus for this first drive inverter design, module FF8MR12W1M1H_B11 is chosen, as Infineon has no modules in stock for a sponsorship during the project work. In laboratory tests later on, the thermal behavior can be investigated and the module can be replaced with the FF8MR12W1M1H_B70 if necessary or when Infineon has the module in stock again.

3.3 Interaction with the Shutdown Circuit

To supply the drivetrain of a Formula Student car with power, the TS battery needs to be connected with the race car. This is done by closing two Accumulator Insulation Relays (AIRs), one relay for each battery pole. The AIRs must be designed in a way, that they are normally opened in a deenergized condition, so that the drivetrain is not electrically connected to its power source. The SDC carries the whole power to drive the AIR coils.

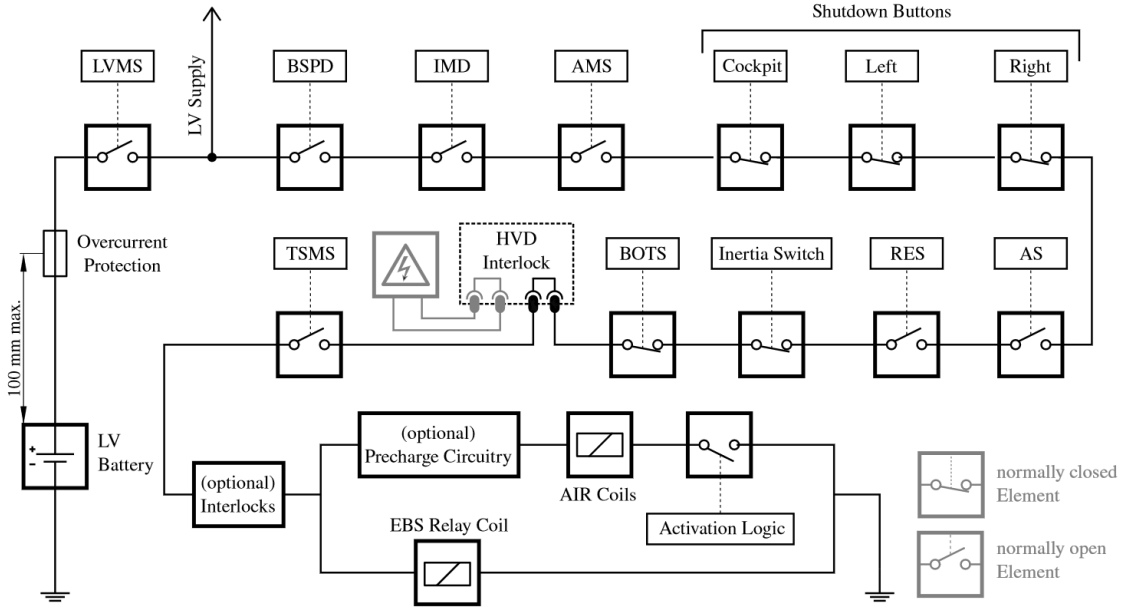


Fig. 3.11: Explanatory schematic of the SDC [7]

An explanatory SDC is depicted in Fig. 3.11. Different safety control units and shutdown buttons (represented by the switch symbols in Fig. 3.11) can open or close the SDC depending on whether they notify a failure (SDC opened) or an absence of failures (SDC closed). The SDC is also responsible for the pre-charge process of the DC link capacitors. The pre-charge circuitry is already implemented in the TS battery, thus such a circuitry does not need to be implemented in the drive inverter.
To enable the opportunity of influencing the SDC via the inverter, a circuitry is implemented, which can open or close the SDC via a semiconductor relay. Additionally, the end of the SDC, which is directly connected to the AIR coils, is also connected to an extra hardwired enable signal for the inverter output stage. Furthermore, this signal controls the discharge circuitry, which connects the poles of the DC link capacitance via a $4.7\,\mathrm{k\Omega}$ resistor. The discharge circuitry must always be active, if the SDC is opened.

3.4 Gate Driver Circuitry

The gate driver circuitry allows greater current capability and lower resistance than the microcontroller pin. Therefore, the microcontroller only generates a controlled PWM signal with a frequency of 20 kHz that is fed to the non-inverting terminal of the gate driver Integrated Circuit (IC). The inverting input is connected to the PWM signal for the other MOSFET of the same halfbridge. The gate driver IC then drives the MOSFET gate using isolated 15 V and −4 V supply, with the connections made according to the datasheet specifications. If both PWM signals are high, the gate driver turns the MOSFET off and thus preventing the halfbridge in a first instance from a short circuit.

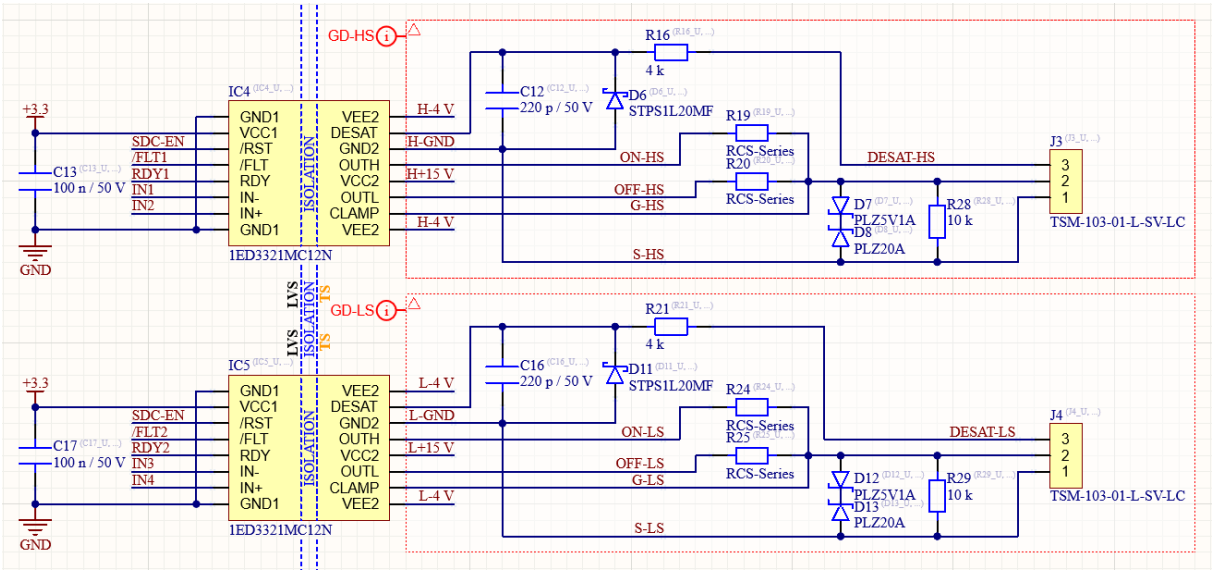


Fig. 3.12: Gate driver circuitry

Fig. 3.12 depicts the schematic of the gate driver circuitry of the system. To protect against transient voltage spikes and unwanted turn-on of the MOSFET, as well as to discharge any accumulated charge on the gate, Zener diodes and a resistor are placed across the gate and source. Additionally, the selected gate driver offers a clamping pin, which directly connects the gate via an internal low-impedance path to the negative power supply of −4 V, if the gate voltage falls below 2 V during turn off. This active miller clamp functionality prevents a turned-off MOSFET from unwanted turn-on during the turn-on of the opposite MOSFET in a half-bridge configuration.
Furthermore, the gate drivers also have an integrated MOSFET overcurrent protection. Through the DESAT pin of the driver, a constant current of $I_{\mathrm{DESAT}} = 510\,\mu\mathrm{A}$ is fed through the channel of the MOSFET, if the driver output is high. An external DESAT diode is connected with a resistor between the DESAT pin of the driver and the drain of the MOSFET. An overcurrent of the MOSFET is detected, if the drain-source voltage is greater than the voltage drop across the external resistor through the constant current I_{DESAT}, as the diode is then in reverse polarity direction. As a result, the measured voltage

at the DESAT pin will increase and activate the short circuit protection. This is also reported via a low /FLT open drain output of the drivers LVS side. If the gate driver has overcurrent detected, it needs to be reset via the /RST pin. The /RST pin is connected to the SDC enable signal. Thus an overcurrent event can only be reset by opening the SDC and closing it again manually. The RDY signal indicates a proper voltage supply and a faultless internal operation of the LVS side of the gate driver. These features ensure the correct and reliable operation of the MOSFET.

3.5 DC Link Circuitry with Voltage Measurement

The DC link circuitry consists of six DC link capacitors selected in section 3.2 so that they can be equally distributed to the three half-bridges. To monitor the DC link voltage, an isolated Delta Sigma Modulator is used. The DC link voltage is connected through a voltage divider to the inputs of the Delta Sigma Modulator, which converts the measured voltage into a bitstream signal on the LVS side, that has to be evaluated in the microcontroller. The Delta Sigma Modulator receives a clock signal with a frequency of up to 20 MHz from the microcontroller.

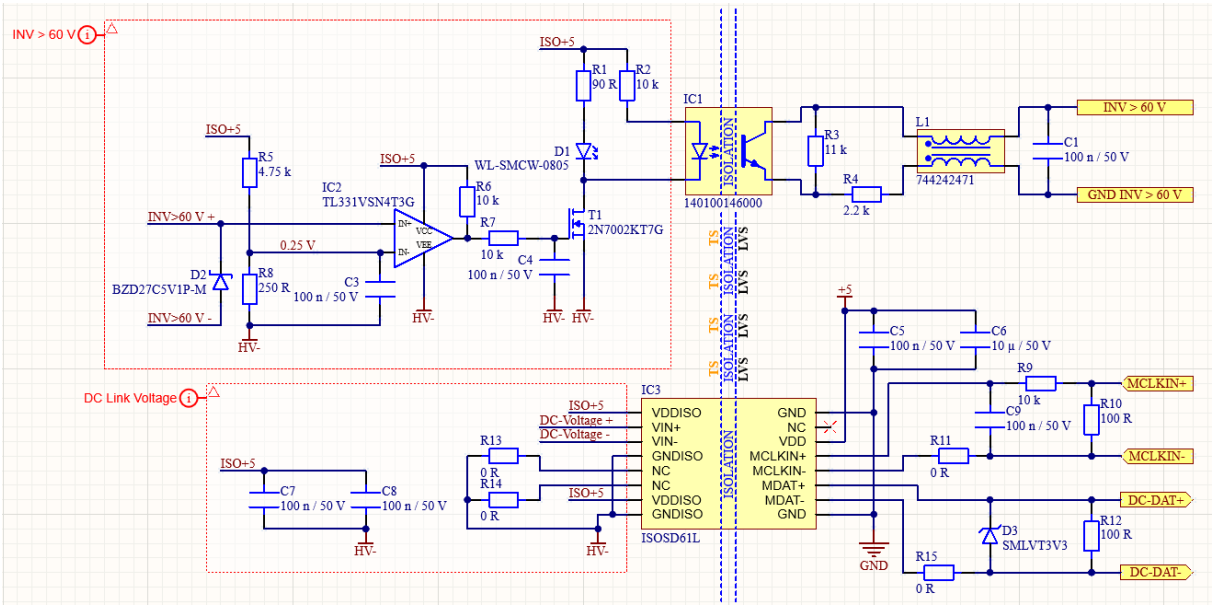


Fig. 3.13: DC link voltage measurement and over 60 V detection

Fig. 3.13 shows beside the DC link voltage measurement the hardwired circuit to detect whether the DC link voltage is greater than 60 V which is required for the illumination of the TSAL (see section 2.1.9). The DC link voltage is also reduced by a voltage divider and then compared with the threshold voltage equal to a reduced DC link voltage of 60 V. When the DC link exceeds 60 V the comparator activates an optocouple which transmits the signal to the LVS side.

3.6 Isolated Gate Driver Power Supply

As a gate driver power supply, an integrated DC-DC converter from Murata is selected. The product line MGJ1 Series, which is shown in Fig. 3.14, offers three bipolar output voltage combination (15 V/−5 V, 15 V/−9 V, 19 V/−5 V) with a nominal input voltage of 24 V [26]. For this inverter a bipolar output voltage of 15 V/−5 V is selected, because the recommended gate source voltage of the chosen MOSFET module is −5 V to 0 V respectively 15 V to 18 V [27].
The DC-DC converter has a power rating of 1 W and is therefore compliant with the requirements formulated in section 3.1.2. Its small size and especially the low profile helps to achieve a compact inverter assembly.

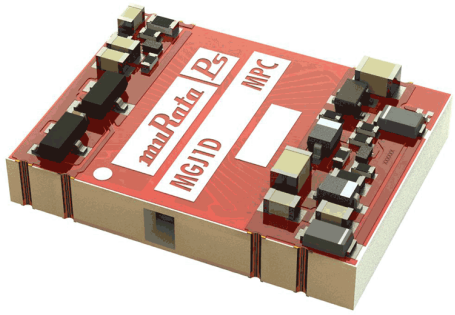


Fig. 3.14: Isolated bipolar output gate driver DC-DC converter [26]

3.7 Phase Current Measurement

To measure the phase currents, which are needed to control the motor (see Fig. 3.1), three hall effect current transducers, as shown in Fig. 3.15, are implemented with a nominal RMS measuring range from $-100\,\mathrm{A_{RMS}}$ to $100\,\mathrm{A_{RMS}}$. They are supplied with unipolar 5 V and have a linear output characteristic. The reaction time is lower than 200 ns, which is around 0.4 % of the switching period $T_{\mathrm{sw}} = 50\,\mu\mathrm{s}$ at $f_{\mathrm{sw}} = 20\,\mathrm{kHz}$. This ensures that the motor can be controlled optimal and fast, as the current signal will be transmitted with a low time delay. The current transducers already have an isolation barrier integrated, so no additional isolation components need to be added between TS and LVS.

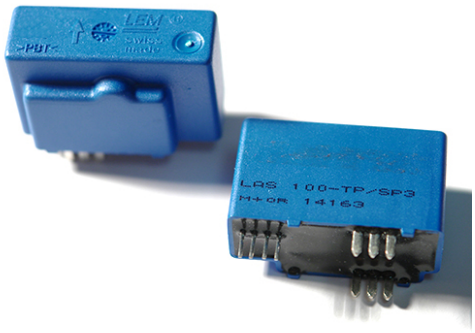


Fig. 3.15: LEM LAS 100-TP [28]

3.8 Discharge Circuitry

As specified in section 2.1.8, the DC link capacitance has to be discharged within 5 s, if the SDC is opened. This is ensured by a discharging circuit which can connect the poles of the DC link via a $R_{\text{Discharge}} = 4.7\,\text{k}\Omega$ resistor with a continuous power rating of 100 W. The time for discharging the DC link from $U_{\text{DC,max}} = 600\,\text{V}$ to $U_{\text{Discharged}} = 60\,\text{V}$ can be calculated to be

$$T_{\text{Discharge}} = -\ln\left(\frac{U_{\text{Discharged}}}{U_{\text{DC,max}}}\right) \cdot R_{\text{Discharge}} \cdot C_{\text{DC}} \tag{3.7}$$

$$= -\ln\left(\frac{60\,\text{V}}{600\,\text{V}}\right) \cdot 4.7\,\text{k}\Omega \cdot 60\,\mu\text{F} \tag{3.8}$$

$$= 649\,\text{ms} \tag{3.9}$$

Even if four inverters are installed in the race car, the discharging time for a total DC link capacitance of 240 µF would be 2.597 s and thus does not exceed the limit of 5 s.

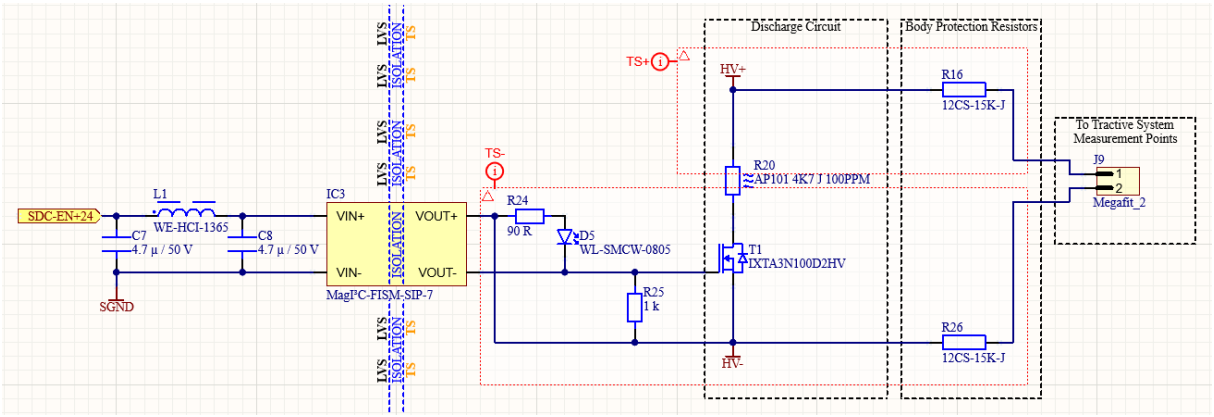


Fig. 3.16: Discharge circuitry

As shown in Fig. 3.16, the discharge circuit is closed by a depletion mode MOSFET. This guarantees that the discharge circuit is normally active and the DC link remains reliably discharged without external actuation. The depletion mode MOSFET is controlled by an isolated DC/DC converter, whose output is high, if the input, which is connected to the SDC enable signal, exceeds 21.6 V, i.e. the SDC is closed, the DC link gets pre-charged and the inverter power electronics are activated.
To measure the DC link voltage outside the inverter and to limit the current through the measurement points in case of a short, two 15 kΩ body protection resistors are installed between each TS pole and its corresponding measurement point.

3.9 PCB Layout

The inverter assembly, which is depicted in Fig. 3.17, is split into four functional groups which have their own PCBs. This helps to reduce the manufacturing cost since the Isolation Board and the Discharge Board have in contrast to the TS Power Board no big requirements regarding their ampacity and thus do not need to have the same layer amount or thickness.

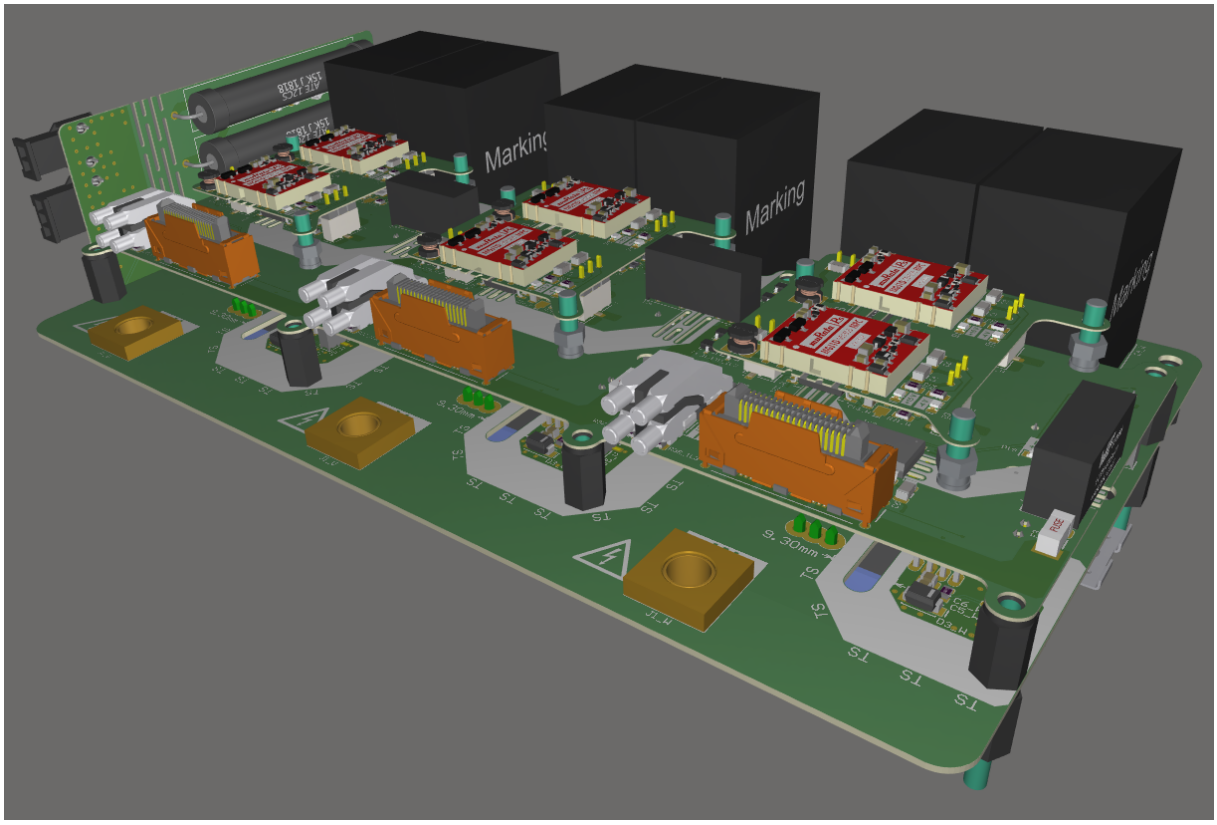


Fig. 3.17: Assembly of the inverter system

The PCBs are arranged in a stack to keep the total assembly space small and to exploit the room beside high components like the DC link capacitors, which would otherwise remain empty. The TS Power Board is the base of the stack and contains the three half-bridge modules the current sensors on the bottom side and the DC link capacitors, which are placed as close as possible to the half-bridges, together with connectors to the Isolation Board on the top side. The TS Power Board is also mounted to a cold plate since the half-bridges need to be actively cooled. The heat sink itself can be mounted to an enclosure.
The Isolation Board contains the gate drivers, the isolation barrier for the temperature measurement of the half-bridges, and the DC link voltage measurement as well as the over 60 V detection together with their isolation barriers. To minimize the resistance and

inductance in the path between the gate driver outputs and the gates of the half-bridges, the board-to-board connectors are placed as close as possible to the corresponding pins of the gate drivers and the half-bridges.
As there are repeating groups of components in the design, e.g. the half-bridges together with the DC link or the gate drivers for the different half-bridges, a room-based design is created so that the component arrangement and the routing can be copied from one room instance to the other ones. This ensures, that the component arrangement is the same for each phase to minimize disturbances caused by an unequal layout, such as increased resistances or inductances.

Tab. 3.4: Clearances between TS nets

	TS+		TS-		Phase		Gate Driver High Side		Gate Driver Low Side	
	IL	EL	IL	EL	IL	EL	IL	EL	IL	EL
TS-	2 mm	4 mm								
Phase	2 mm	4 mm	2 mm	4 mm	2 mm	4 mm				
Gate Driver High Side	2 mm	4 mm	2 mm	4 mm	2 mm	4 mm				
Gate Driver Low Side	2 mm	4 mm	1 mm	2 mm	2 mm	4 mm	2 mm	4 mm		
Temperature & DC Link Voltage Measurement	2 mm	4 mm	2 mm	4 mm	2 mm	4 mm	2 mm	4 mm	1 mm	2 mm

Due to the high maximum TS voltage, it must be paid attention to sufficient spacing between TS nets. The distances are calculated according to IPC-2221 [29]. As transient processes can lead to higher voltage sparks, a voltage of 1200 V is assumed. For Internal Layers (ILs), IPC-2221 recommends a spacing of 2 mm. For External Layers (ELs) with conformal coating, a minimum spacing of 2.935 mm is necessary.
Tab. 3.4 shows the clearances between the different TS nets checked by the design rules. Since the low side gate drivers and the temperature measurement are referenced to TS- potential, theoretical no spacing between these nets is necessary. However, a spacing of 1 mm in ILs and 2 mm in ELs is maintained to separate the functional parts as much as possible while enabling a compact PCB design.
To carry the currents of the power electronics, the copper thicknesses of the TS Power Board need to be calculated. According to IPC-2221 [29], the maximum ampacity can be calculated by

$$I_{\mathrm{Cu,max}} = k \cdot \Delta\vartheta^{0.44} \cdot A^{0.725} \tag{3.10}$$

where k is equal to $k_{\mathrm{IL}} = 0.024$ for ILs and equal to $k_{\mathrm{EL}} = 0.048$ for ELs. $\Delta\vartheta$ is the maximum temperature increase in Kelvin of the considered layer and A is the layer cross-section in sq. mils. A motor current analysis from logging data of the UPBracing Team during a high-speed race shows, that the RMS motor current during this race

was $I_{\mathrm{Cu,RMS}} = 32\,\mathrm{A_{RMS}}$. With this RMS current, a maximum temperature increase of $\Delta\vartheta = 35\,\mathrm{K}$, that is reached for a layer temperature of 70 °C at an ambient temperature of 35 °C (see section 3.1.2) and a layer thickness of $d_{\mathrm{Cu}} = 105\,\mu\mathrm{m} \equiv 4.13\,\mathrm{mils}$, the necessary track width $W_{\mathrm{Cu,min}}$ can be calculated with Eq. 3.10 to

$$W_{\mathrm{Cu,min}} = \sqrt[0.725]{\frac{I_{\mathrm{Cu,RMS}}}{k_{\mathrm{IL}} \cdot \Delta\vartheta^{0.44}}} \cdot \frac{1}{d_{\mathrm{Cu}}} \tag{3.11}$$

$$= \sqrt[0.725]{\frac{32\,\mathrm{A_{RMS}}}{0.024 \cdot 35\,\mathrm{K}}} \cdot \frac{1}{4.13\,\mathrm{mils}} \tag{3.12}$$

$$\approx 571.77\,\mathrm{mils} \equiv 14.5\,\mathrm{mm} \tag{3.13}$$

The TS- and TS+ nets are each routed on two layers. The minimum track width for one layer is than $W_{\mathrm{Cu,min,Layer}} = 7.25\,\mathrm{mm}$.

4 Summary and Outlook

During this master project, the power electronics for a drive inverter for racing applications of the UPBracing Team is designed and developed. The design is compliant to the Formula Student Regulations 2024 v1.1, achieves a slightly smaller assembly space (length x width x height: 20 cm x 12 cm x 6 cm) and is more lightweight than the previously used and purchased inverter of the UPBracing Team due to the significantly lower weight of the MOSFET modules compared with the IGBT module.
The development bases on power loss analyses of different SiC MOSFET modules, from which the most efficient one is selected. The power loss analyses also clarify, that the RMS current method has a better cost-benefit ratio than the Modulation method with respect to a fast power loss estimation, but overestimates the losses by around 30 % compared with the IPOSIM simulation, which is considered as most realistic.
The project sets the basis for further development of the drive inverter design. Especially the validation of the power loss analyses and the thermal performance of the half-bridge modules needs to be done subsequently. Additionally, the optimal gate driver resistors need to be selected due to laboratory tests. Beside this, the next step is to set up a motor control, complete the inverter hardware with a Control Board, implement the controller in the design, start testing and optimizing the system iterative.

Appendix

A.1 Altium Designs

Isolation Board (SiC_Inverter_PX4FuturE_GD-Isolation):
Project: SiC_Inverter_PX4FuturE_GD-Isolation.PrjPcb
Schematics:
- Top.SchDoc
  - DC-Link.SchDoc
  - Isolated_LV_Power.SchDoc
  - Gate-Driver_Circuit.SchDoc
    - Temperature-Measurement.SchDoc
    - RGB-LED_Indication.SchDoc

PCB: Gate-Driver_Isolation.PcbDoc

Gate Driver Power Board (SiC_Inverter_PX4FuturE_GD-Power_Murata):
Project: SiC_Inverter_PX4FuturE_GD-Power_Murata.PrjPcb
Schematic: GD-Power_Murata.SchDoc
PCB: GD-Power_Murata.PcbDoc

TS Power Board (SiC_Inverter_PX4FuturE_TS-Power):
Project: SiC_Inverter_PX4FuturE_TS-Power.PrjPcb
Schematics:
- Top_TS-Power.SchDoc
  - DC-Link_Halfbridge_Current-Sensor.SchDoc
  - DC-Link-Measurement.SchDoc

PCB: TS-Power.PcbDoc

Discharge Board (SiC_Inverter_PX4FuturE_TS-Discharge):
Project: SiC_Inverter_PX4FuturE_TS-Discharge.PrjPcb
Schematics:
- Top_TS-Discharge.SchDoc
  - Discharge.SchDoc
  - 60V-Detection.SchDoc

PCB: TS-Discharge.PcbDoc

Inverter Assembly (SiC_Inverter_PX4FuturE_Assembly):
Project: Inverter_Assembly.PrjMbd
Schematic: Inverter_Assembly.MbsDoc
Assembly: Inverter_Assembly.MbaDoc

Libraries (SiC_Inverter_PX4FuturE_Library):
Schematic Library: SiC_Inverter_PX4FuturE_SchLib.SchLib
PCB Library: SiC_Inverter_PX4FuturE_PcbLib.PcbLib

Lists

Acronyms

AC Alternating Current

AIR Accumulator Insulation Relay

BJT Bipolar Junction Transistor

CAN Controller Area Network

DC Direct Current

EL External Layer

ESR Equivalent Series Resistance

EV Electric Vehicle

HEV Hybrid Electric Vehicle

HVDC High Voltage Direct Current

IC Integrated Circuit

IGBT Insulated Gate Bipolar Transistor

IL Internal Layer

JFET Junction Field-Effect Transistor

LVS Low Voltage System

MLCC Multi Layer Ceramic Capacitor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

PCB Printed Circuit Board

PMSM Permanent Magnet Synchronous Motor

PWM Pulse Width Modulation

RMF Rotating Magnetic Field

RMS Root Mean Square

SCS System Critical Signal

SDC Shutdown Circuit

SiC Silicon Carbide

TS Tractive System

TSAL Tractive System Active Light

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