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Leistungselektronik und
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Prof. Dr.-Ing. Joachim Böcker

Paderborn University
Faculty for Computer Science, Electrical Engineering and Mathematics
Department Power Electronics and Electrical Drives (LEA)

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DESIGN OF A 4 TIMES INTERLEAVED 2 KW AUTOMOTIVE DC-DC CONVERTER

by:	Marius Becker	beckerm3@mail.uni-paderborn.de
	Ishani Engineer	ishani@mail.uni-paderborn.de
	Jan Wiegard	jwiegard@mail.uni-paderborn.de
	Denis Zeinel	zeinel@mail.uni-paderborn.de

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examiner: Prof. Dr.-Ing. Joachim Böcker
advisors: Philipp Rehlaender, Nikolas Förster

Contents

1. Introduction **1**

1.1. Task Description 1

2. Thermal Simulation of the PCB **4**

2.1. Theoretical Calculation of the Temperatures 5

2.2. Simulation with Vias Replacing Material 8

2.3. Simulation with Filled Vias 10

2.4. Simulation with Unfilled Vias 12

2.5. Simulation with Unfilled Vias and all PCB Layers 13

2.6. Comparison of the Different Simulation Models and Future Improvements of the Simulation 16

3. Inductor Simulation **19**

3.1. Optimization 19

3.2. Core Loss Calculation 20

3.3. Simulation Procedure Transient Analysis 23

3.4. Simulation Results 25

3.5. Conclusion 27

4. Housing **29**

4.1. Requirements 29

4.2. Design of the Housing 30

4.3. Conclusion 34

5. Inductor Build-Up **35**

5.1. Design of the Footprint 35

5.2. Basic Production Steps 36

5.2.1. Winding 36

5.2.2. Ferrite 38

5.2.3. Air Gap 40

5.2.4. Measurement 41

5.3. Conclusion and Outlook 46

6. Overview of the Cascade Control of the DC/DC Converter **47**
6.1. Cascade Control 47
6.2. Implementation of the Cascade Control on the Microcontroller 49
6.3. Firmware 50

7. Hardware Tester **52**
7.1. Hardware Tester Firmware 52

8. Altium-Library **53**
8.1. Creation of New Components 53

9. Measurements of Version 10 Converter **56**
9.1. Experimental Setup 56
9.2. Implementation 58
9.3. Evaluation 59

10. Description of the WS19/20 DC/DC Board Version 10.0 Errata **61**
10.1. Missing Connections 63
10.2. Error in the Footprint of the MOSFET 65
10.3. Error in JTAG Footprint 69
10.4. Problems Current Measurement 69
10.5. Problems with the Coupled Inductors 71
10.6. Problem Short Circuit during Programming 71
10.7. Remark at the New Layout of the Board Version 10.0 72

11. Description of the WS20/21 DC/DC Board Version 11.0 Errata **73**
11.1. ADC Inputs 74
11.2. Error Control Card Connector 74
11.3. Remark at the New Layout of the Board Version 11.0 75

12. Abstract **76**

A. Appendix **78**
A.1. Ansys Electromagnetic Simulation - Configuration List 78
A.2. Matlab Code for the Geometry Generation 80

Bibliography **82**

List of Figures

1.1. 3D representation of the converter PCB as well as inductor placement. . . 2
1.2. PCB layout of the 2 kW converter (top view) 2

2.1. Thermal equivalent circuit diagram of the PCB in steady-state 6
2.2. Principal geometry of the simulation model with vias replacing material (top: side view, bottom: top view) 9
2.3. Results of the thermal simulation with vias replacing material 9
2.4. Principal geometry of the simulation model with filled vias (top: side view, bottom: top view) 11
2.5. Results of the thermal simulation with filled vias 11
2.6. Principal geometry of the simulation model with unfilled vias (top: side view, bottom: top view) 12
2.7. Results of the thermal simulation with unfilled vias 13
2.8. Principal geometry of the simulation model with unfilled vias and all PCB layers (top: side view, bottom: top view) 14
2.9. Results of the thermal simulation with unfilled vias and all PCB layers . . 15

3.1. Transient simulation: Core loss vs Time 22
3.2. Transient simulation: Copper loss vs Time 23
3.3. Excitation current in the Simulation. 24
3.4. General simulation workflow on Ansys-Electronics Desktop 24
3.5. Losses and $B_{\max}$ vs parametric variations (logarithmic scale) 26
3.6. Losses vs parametric variations 27
3.7. AC and DC ohmic loss content in the total ohmic loss in various configurations of the inductor topology 28

4.1. Bottom of the housing with the liquid path. The red arrows show the drilling holes 31
4.2. Top of the bottom part with the pedestals for the thermal connection between housing and PCB 31
4.3. SAE J2044 fitting from Parker [11] 32

4.4. AMP+HVP800 connector from TE [13] 32
4.5. Outside the housing 33
4.6. Inside the housing 33

5.1. 3D-Print from the cuboid and cylinder as a model of the ferrite parts . . . 36
5.2. Model of the inductor with connection to the PCB (footprint) 37
5.3. The basic inductor components: winding, air gap material and ferrite core 37
5.4. Broken copper on the marked area due to mechanical stress during the winding process 39
5.5. Arrangement in the U-Core 39
5.6. Arrangement in the cuboid from HELENE 42
5.7. The white air gap material is visible at the surface between the cuboid and the cylinder 42
5.8. The Aluminium Oxide Ceramic plate for the TO-case before and after the milling process 43
5.9. A nearly finished inductor with attached ceramics. One ferrite cuboid must be added 43
5.10. Plot of the measured inductors 44
5.11. The two ceramic plates are removed and Kapton tape is added. Two extensions are soldered to he inductor to enable a connection to the impedance analyser. 45
5.12. Here a finished inductor is shown. 45

6.1. Block diagram of the four times interleaved cascade control for the DC/DC converter 47
6.2. Block diagram of inner current control 48
6.3. Block diagram from outer voltage control 49
6.4. Concept of the Hardware Abstraction Layer (HAL) 50

8.1. Footprint Wizard window in Altium 54
8.2. Example of footprint with labeling on layer 29 55
8.3. Example of parameter setting of components 55

9.1. The experimental setup in the lab. 57
9.2. Experimental setup of version 10 DC/DC-converter as Device under Test (DUT). 57
9.3. Efficiency of the DC/DC converters 60

10.1. DC/DC Converter Ver. 10.0 PCB 61

10.2. DC/DC Converter Ver. 10.0 with heat sink 62
10.3. Missing ground connection for the voltage divider 63
10.4. Missing connection to the output voltage from the converter for the status LED 64
10.5. Missing connection to output voltage of converter for current measurement of rail 2 65
10.6. Manufacturer recommendation for MOSFET footprint 66
10.7. Too small distance between drain pad and thermal pad 67
10.8. Footprint MOSFET version 10.0 with errors 67
10.9. Footprint MOSFET version 10.0 corrected 68
10.10Half-bridge midpoint voltage with incorrectly positioned high-side MOSFET 68
10.11Half-bridge midpoint voltage with same high-side MOSFET but correct positioning 69
10.12JTAG footprint with swapped sides 70
10.13JTAG connection destroyed 70

11.1. DC/DC Converter Ver. 11.0 PCB 73
11.2. Control Card Footprint error 75

List of Tables

2.1. Quantities of the different regions for the calculation of the thermal resistances 6
2.2. Structure of the PCB and thicknesses of the layers 14
2.3. Maximum temperatures of the inductor, the low-side and high-side MOSFET calculated theoretically and with different simulation models, simulation time (without meshing) and number of grid cells of the simulation models 17

3.1. Results from Optimetrics analysis on Ansys 20
3.2. Configuration with lowest total loss as given in Figure 3.6 26

4.1. Comparison of power density and volume of the different converters 34

5.1. Comparison of the different ferrite materials Fi395 [17] and N95 [15] 40

9.1. Quantities of the different regions for the calculation of the thermal resistances 59
9.2. Configuration with lowest total loss 60

A.1. Configurations and their respective labels A 78
A.2. Configurations and their respective labels B 79

1. Introduction

Due to stricter CO_2 emission limits as well as the increased comfort requirements (e.g. steer-by-wire) in automobiles lead to an increased power demand. A 48 V supply is used to meet this increased power demand. The 12 V voltage supply is still required for compatibility with existing 12 V consumers. To transfer electrical energy efficiently, cost-effectively and compactly between both voltage levels, a DC/DC converter can be used. By using a DC/DC converter, the 12 V battery can be reduced or eliminated entirely.

1.1. Task Description

Previous projects focused on design and optimization of 1 kW bidirectional 48 V to 12 V DC/DC converter. In summer semester 2020 a new converter of 2 kW is designed [1] (see Figure 1.1 and Figure 1.2). The goal of this project is to complete the design of the 2 kW and further optimize the new converter. The PCB layout has been completed by this project group, but was described in detail in the previous project report [1].

An important task in winter semester 2020/21 is the thermal analysis of the PCB, especially the estimation of junction temperature rise of the chosen Si-MOSFET. Since these are the critical components of the converter circuit, junction temperature rise is an important parameter in deciding the cooling strategy to be used in the converter to avoid damage of sensitive components and to prevent localized hot-spots in the PCB. Further, in depth explanation regarding the simulation procedure can be found in Chapter 2. The new magnetic topology developed in the previous semester needed further optimization.

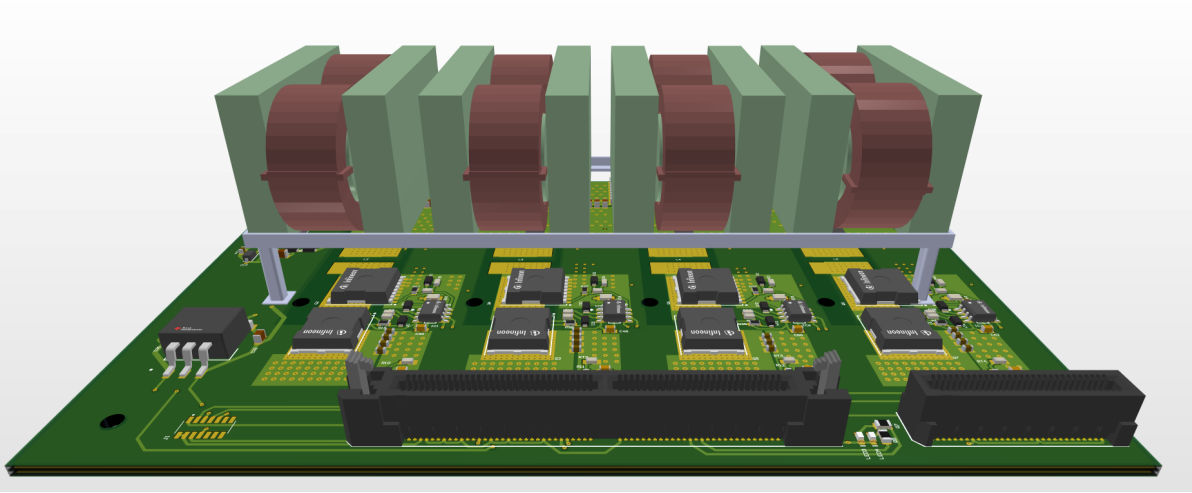

Figure 1.1.: 3D representation of the converter PCB as well as inductor placement.

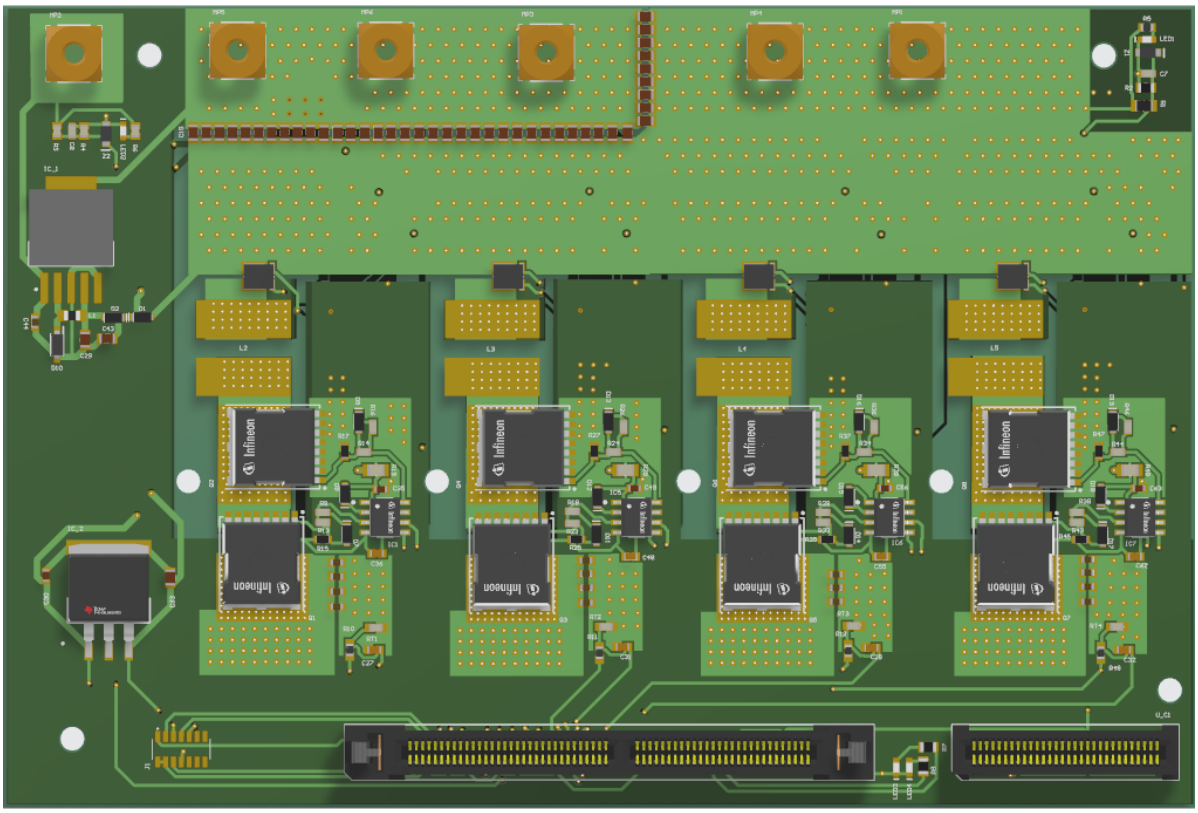

Figure 1.2.: PCB layout of the 2 kW converter (top view)

A different simulation strategy for the optimization of the magnetic topology is tested in this project. In-depth information about the simulation procedure can be found in Chapter 3.

Construction and design of mechanical housing along with the liquid cooling system is important for the heat dissipation of the converter. Because the converter is designed for automobile application, the respective design standard is kept in mind during designing the housing. The design and construction of the mechanical housing is explained thoroughly in Chapter 4. A new control card was chosen in the previous semester so the complete code needs to be developed for the new microcontroller. Further details are explained in Chapter 6.

The new 2 kW (version 11.0) converter is built-up along with the testing of the old 1 kW (version 10.0) converter in this project. A detailed explanation regarding the build-up and testing process can be found in Chapter 9. The problems encounter during the built-up of the 1 kW and 2 kW converter are explained in detail in Chapter 10 and Chapter 11.

2. Thermal Simulation of the PCB

This chapter deals with the thermal simulation of the 2 kW DC/DC converter from WS 2020/21 (version 11.0). At first, a theoretical calculation of the maximum temperatures based on a thermal equivalent circuit diagram is done to have a result that can be compared with the simulation results that are presented afterwards. For the simulations the open source software *Sparselizard* is used the first time because it is a code-based C++ FEM tool what makes it user friendly. Here, four different models of the PCB are investigated with regard to accuracy and model complexity. Since the thermal vias are the most complex elements of the geometry, only they are modeled differently:

1) The thermal vias are replaced by a homogenous material with the same thermal resistance. The PCB layers are neglected.

2) The thermal vias are modeled as solid cylinders without a hole in it. The PCB layers are neglected.

3) The thermal vias are modeled as cylinders with a hole in it. The PCB layers are neglected.

4) The thermal vias are modeled as cylinders with a hole in it and all PCB layers are contained in the model.

The objective of this investigation is to find out which model complexity is needed to achieve accurate results. For the assessment of the model complexity the simulation time and the number of grid cells of the meshes are compared. The temperature distribution in the inductor and MOSFETs themselves is not calculated.

In the end, all the results are compared to each other and to the maximum junction temperature $T_{\mathrm{j,max}} = 175\,^{\circ}\mathrm{C}$ of the used MOSFETs [2]. Furthermore, the differences of the resulting temperatures between the models are explained and a conclusion is made.

2.1. Theoretical Calculation of the Temperatures

The structure of the PCB is shown in Figure 1.2 (see chapter 4 in [1] for more details). Due to the distances between the four rails, only one rail is simulated and the results apply to all rails. The heat sources are the inductor which has two thermal conduction paths, the low-side MOSFET which uses one of the thermal conduction paths of the inductor and the high-side MOSFET that utilizes another path.

The thermal equivalent circuit diagram looks like depicted in Figure 2.1. For the thermal calculation only the copper contacts on the PCB are considered (represented by $R_{\mathrm{th,Ind,cont}}$ and $R_{\mathrm{th,Tr,cont}}$) since they connect the electrical devices with the thermal vias. The copper layers of the PCB are neglected due to the small thermal conductivity of the insulation material between them. After the copper contacts the heat flows through the thermal vias ($R_{\mathrm{th,vias1-3}}$) to the thermal interface material (TIM, $R_{\mathrm{th,TIM1-3}}$) and then to the heatsink. For the MOSFETs the thermal resistance from junction to case R_{thjc} has to be considered additionally. The heatsink is assumed to be a perfect thermal conductor whose temperature is the ambient temperature T_{a} since it is not designed yet.

The produced losses of the inductor are $P_{\mathrm{loss,Ind}} = 3\,\mathrm{W}$ [1], the losses of the low-side MOSFET are $P_{\mathrm{loss,Tr,low}} = 3.5\,\mathrm{W}$ and of the high-side MOSFET $P_{\mathrm{loss,Tr,high}} = 6\,\mathrm{W}$ [1]. The ambient temperature is assumed to be $T_{\mathrm{a}} = 60\,^{\circ}\mathrm{C}$ which corresponds to the temperature of the liquid of the water cooling.

The first step is to determine the thermal resistances of the different conduction paths via the formula [3]

$$R_{\mathrm{th}} = \frac{l}{\lambda A} \tag{2.1}$$

where l is the length of the conduction path, λ is the thermal conductivity of the

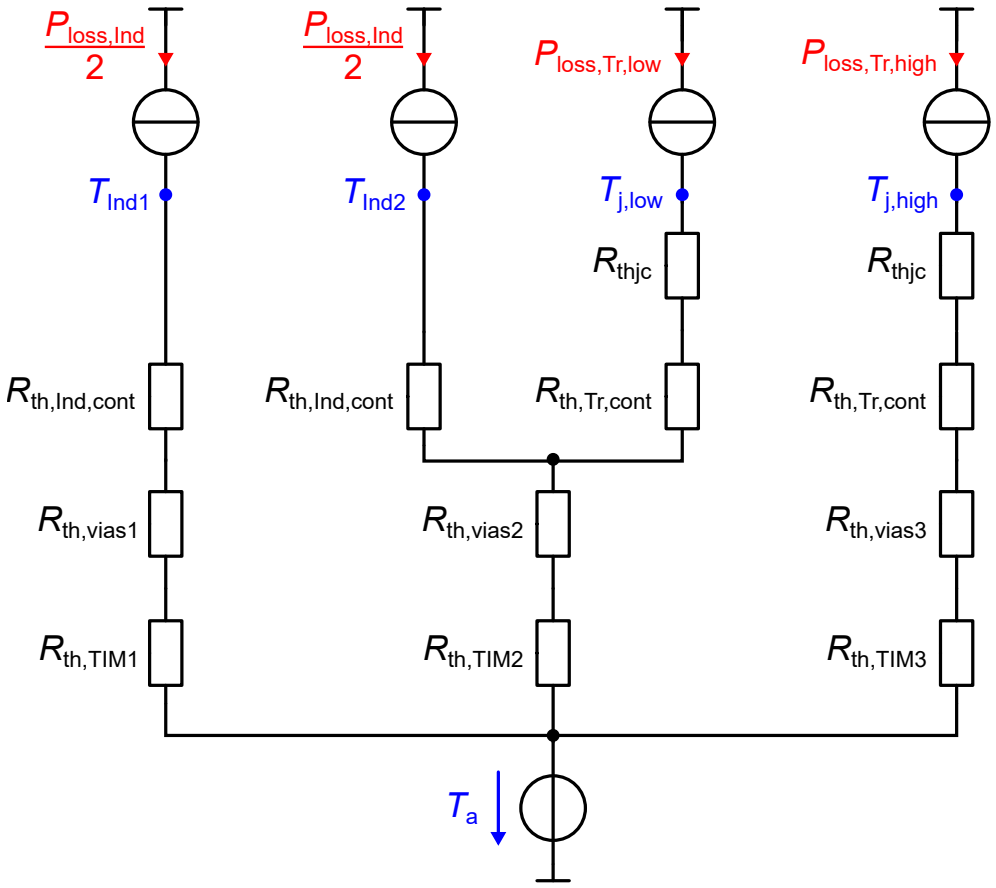

Figure 2.1.: Thermal equivalent circuit diagram of the PCB in steady-state

	l in mm	A in mm^2	λ in $\frac{\mathrm{W}}{\mathrm{Km}}$	R_{th} in $\frac{\mathrm{K}}{\mathrm{W}}$
R_{thjc}	1	36	39.68	0.7
$R_{\mathrm{th,Ind,cont}}$	0.1	42.24	401	0.0059
$R_{\mathrm{th,Tr,cont}}$	0.1	76.13	401	0.0033
$R_{\mathrm{th,vias1}}$	1.5	9.4012	401	0.3979
$R_{\mathrm{th,vias2}}$	1.5	46.7449	401	0.0800
$R_{\mathrm{th,vias3}}$	1.5	47.7895	401	0.0783
$R_{\mathrm{th.TIM1}}$	0.5	96.80	5	1.0331
$R_{\mathrm{th,TIM2}}$	0.5	190.08	5	0.5261
$R_{\mathrm{th,TIM3}}$	0.5	243.22	5	0.4112

Table 2.1.: Quantities of the different regions for the calculation of the thermal resistances

section and A is the cross section through which the heat flows. The given quantites of each region and the calculated resistances are presented in Table 2.1 where the thermal resistance R_{thjc} from junction to case of the MOSFET is already given by the data sheet [2] and its thermal conductivity λ is calculated for the simulations later. The cross section of the thermal vias results from the number of considered vias in the respective region. For $R_{\mathrm{th,vias1}}$ 36 vias are considered, for $R_{\mathrm{th,vias2}}$ 179 and for $R_{\mathrm{th,vias3}}$ 183 (see also Figure 1.2). The outer diameter of the vias is 0.65 mm and the inner diameter (diameter of the holes) is 0.3 mm so the cross section of each single via results in $A_{\mathrm{via}} = 0.2611\,\mathrm{mm}^2$. The hole consisting of air is neglected since it has a low thermal conductivity.

In the next step, the maximum temperatures of the devices can be calculated where T_{Ind1} and T_{Ind2} are the temperatures of the inductor (left and right path), $T_{\mathrm{j.low}}$ is the junction temperature of the low-side MOSFET and $T_{\mathrm{j,high}}$ of the high-side one:

$$
\begin{aligned}
T_{\mathrm{Ind1}} &= (R_{\mathrm{th,Ind,cont}} + R_{\mathrm{th,vias1}} + R_{\mathrm{th,TIM1}}) \cdot \frac{P_{\mathrm{loss,Ind}}}{2} + T_{\mathrm{a}} = 62.2\,^{\circ}\mathrm{C} \\
T_{\mathrm{Ind2}} &= (R_{\mathrm{th,Ind,cont}} + R_{\mathrm{th,vias2}} + R_{\mathrm{th,TIM2}}) \cdot \frac{P_{\mathrm{loss,Ind}}}{2} \\
&\quad + (R_{\mathrm{th,vias2}} + R_{\mathrm{th,TIM2}}) \cdot P_{\mathrm{loss,Tr,low}} + T_{\mathrm{a}} = 63.0\,^{\circ}\mathrm{C} \\
T_{\mathrm{j,low}} &= (R_{\mathrm{thjc}} + R_{\mathrm{th,Tr,cont}} + R_{\mathrm{th,vias2}} + R_{\mathrm{th,TIM2}}) \cdot P_{\mathrm{loss,Tr,low}} \\
&\quad + (R_{\mathrm{th,vias2}} + R_{\mathrm{th,TIM2}}) \cdot \frac{P_{\mathrm{loss,Ind}}}{2} + T_{\mathrm{a}} = 65.5\,^{\circ}\mathrm{C} \\
T_{\mathrm{j,high}} &= (R_{\mathrm{thjc}} + R_{\mathrm{th,Tr,cont}} + R_{\mathrm{th,vias3}} + R_{\mathrm{th,TIM3}}) \cdot P_{\mathrm{loss,Tr,high}} + T_{\mathrm{a}} = 67.2\,^{\circ}\mathrm{C}.
\end{aligned}
$$

From Table 2.1 it can be seen that the thermal resistances of the TIMs are larger than the other resistances so the temperature rises across those dominate over the others. Furthermore, it can be seen that the temperature rise of each device is not very high and the MOSFETs are far away from the critical junction temperature of 175 °C. But it has to be noted that this calculation does not consider any 2D and 3D effects in the heat distribution. In reality, the heat flows through a smaller cross section which increases the thermal resistances. Hence, thermal 3D simulations are done in the following sections to obtain more accurate results.

2.2. Simulation with Vias Replacing Material

In this simulation model the thermal vias are replaced by boxes of homogeneous materiales (see Figure 2.2) which have the same theoretical thermal resistance as the vias in Table 2.1. The reason for this is that this geometry is very easy to implement in *Sparselizard*. Therefore, the thermal conductivities of the three regions that are used in the simulation are calculated with Equation 2.1:

$$\lambda_{\text{vias},1} = \frac{1.5\,\text{mm}}{0.3979\,\frac{\text{K}}{\text{W}} \cdot 96.8\,\text{mm}^2} = 38.94\,\frac{\text{W}}{\text{mK}}$$
$$\lambda_{\text{vias},2} = \frac{1.5\,\text{mm}}{0.08\,\frac{\text{K}}{\text{W}} \cdot 172.8\,\text{mm}^2} = 108.51\,\frac{\text{W}}{\text{mK}}$$
$$\lambda_{\text{vias},3} = \frac{1.5\,\text{mm}}{0.0783\,\frac{\text{K}}{\text{W}} \cdot 243.22\,\text{mm}^2} = 78.76\,\frac{\text{W}}{\text{mK}}$$

For the cross sections of the boxes, the values of the TIMs that connect the PCB to the heatsink are taken. The three regions *vias1*, *vias2* and *vias3* in Figure 2.2 are considered to be decoupled since the thermal vias conduct the heat vertically.

The inductor and the MOSFETs are modeled as boxes of 0.1 mm thickness that produce the power losses (red boxes in Figure 2.2). Their material is chosen as copper like the contacts under them to influence the temperature distribution as little as possible.

One half of the power losses of the inductor flows through the left path and the other through the middle path. The thermal resistances R_{thjc} from junction to case that are below the MOSFETs have the thermal conductivity calculated in Table 2.1 as well as the TIM and the copper layers and contacts. The values of the power losses and the ambient temperature are the same as in Section 2.1. Here, the heatsink is assumed to be a perfect thermal conductor, too.

This geometry is the easiest model of all in this report to implement in *Sparselizard*. Its mesh contains the smallest number of grid cells which is 22,936 after one refinement here and, hence, the simulation time is with $t_{\text{sim}} = 18\,\text{s}$ the smallest of all, too.

The simulation results are presented in Figure 2.3. One can see that the inductor

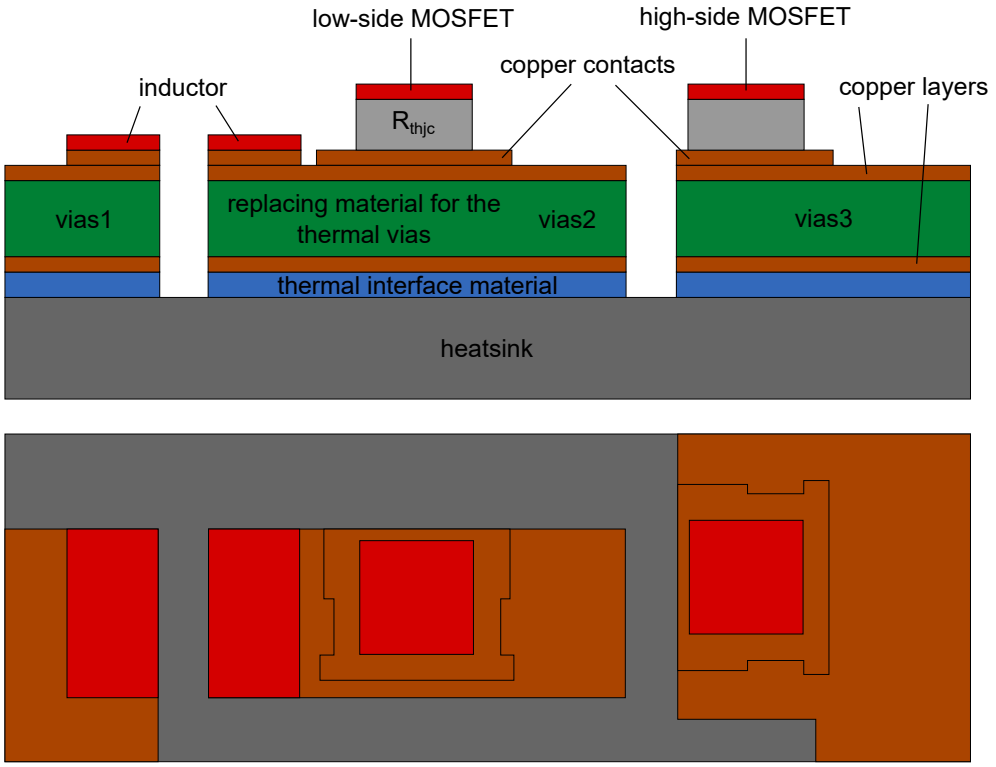

Figure 2.2.: Principal geometry of the simulation model with vias replacing material (top: side view, bottom: top view)

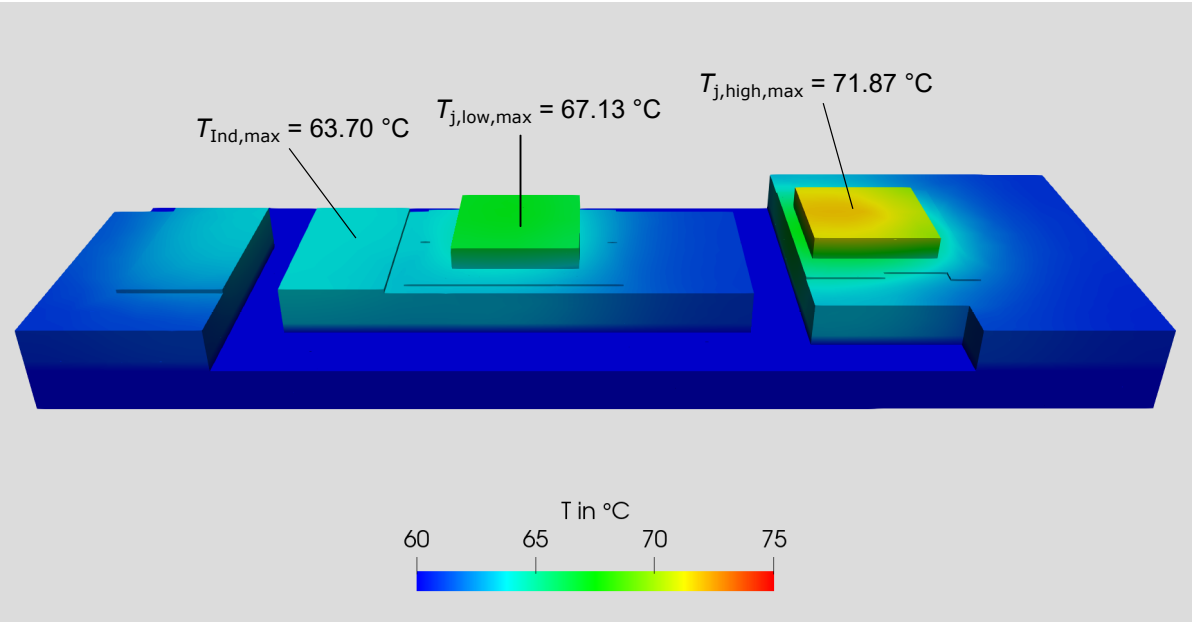

Figure 2.3.: Results of the thermal simulation with vias replacing material

has the lowest temperature with 63.70 °C in comparison with the MOSFETs and the high-side MOSFET becomes hotter than the low-side one. However, the maximum temperature of 71.87 °C is significantly below the maximum allowed junction temperature of 175 °C according to the datasheet [2].

2.3. Simulation with Filled Vias

The next simulation model does not replace the thermal vias by a homogeneous material but they are modeled as solid cylinders of copper as depicted in Figure 2.4. In reality, the vias have holes in it so they are actually not filled with copper. However, the holes are neglected in this geometry to keep the model easy which simplifies the generation of the geometry in *Sparselizard*. After one refinement the mesh contains 305,328 grid cells which is roughly 13 times more in comparison to the mesh of the previous model so more calculations are needed to be done.

The number of vias in Figure 2.4 does not correspond to the used number in the simulation since it only shows the principal and not the exact simulation model. The simulation contains 36 vias under the left inductor contact, 179 under the right inductor contact and low-side MOSFET and 183 under the high-side MOSFET like in Section 2.1. This high number of cylinders that has to be generated is done with the *fprintf* command in Matlab (see Appendix A.2) which makes this geometry a bit more difficult to implement in comparison to the previous geometry but it is still easy nevertheless.

The results in Figure 2.5 show that the temperature rise is mainly caused by the TIM and the thermal resistances R_{thjc}. The maximum temperatures of the devices are only slightly higher than in the simulation in Section 2.2 and, thus, there is a high margin between the critical junction temperature and the simulated ones. However, the simulation time $t_{\text{sim}} = 286\,\text{s}$ is higher due to a higher number of grid cells.

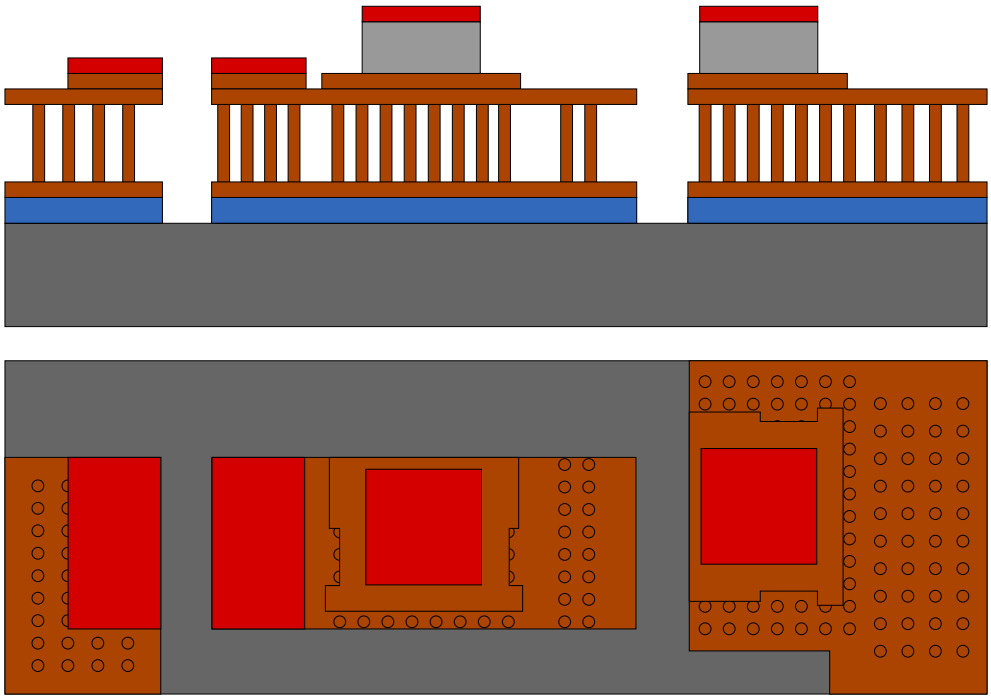

Figure 2.4.: Principal geometry of the simulation model with filled vias (top: side view, bottom: top view)

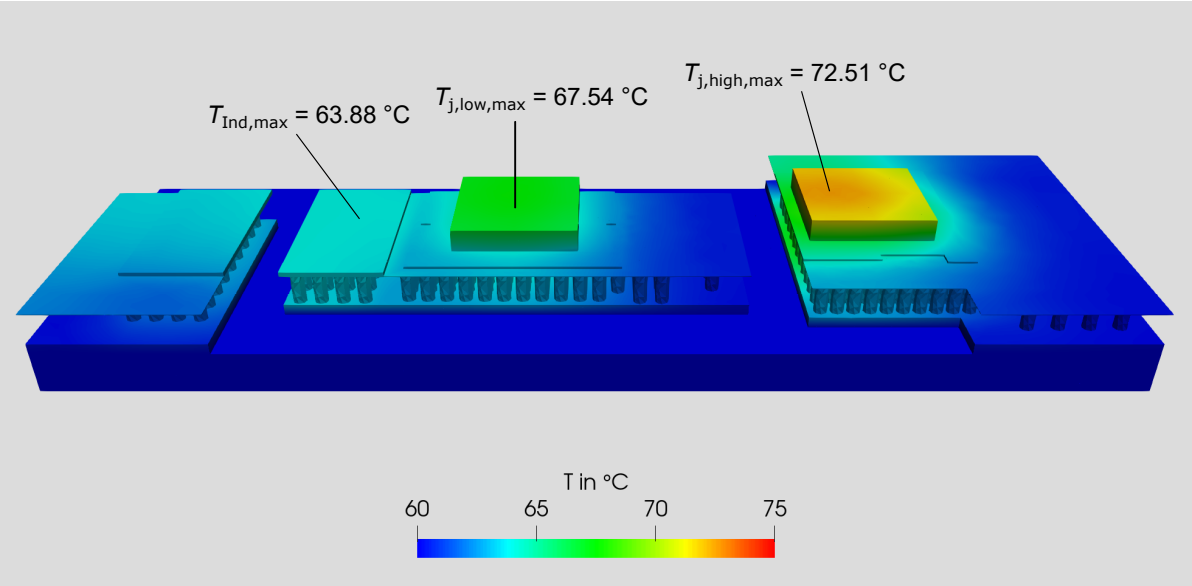

Figure 2.5.: Results of the thermal simulation with filled vias

2.4. Simulation with Unfilled Vias

A further improvement of the simulation is to add the holes in the thermal vias like in Figure 2.6. This makes the simulation more accurate on the one hand but, on the other hand, the geometry becomes more complex with respect to its generation and the computational effort is higher because a higher number of grid cells is necessary to model the small holes. The holes were not put in the top and bottom PCB layer because this results in a higher effort in modelling the geometry in *Sparselizard* (see [4] for more details regarding modelling). Furthermore, this would not have a big influence on the results because of the small thickness of 0.035 mm of the outer layers. As previously, Matlab was used for the generation of the thermal vias and their holes in the simulation model (similar to the code in Appendix A.2). The mesh is refined once resulting in 562,136 grid cells which is a bit higher than without holes inside the vias. The same applies to the simulation time which increases to $t_{\text{sim}} = 504\,\text{s}$.

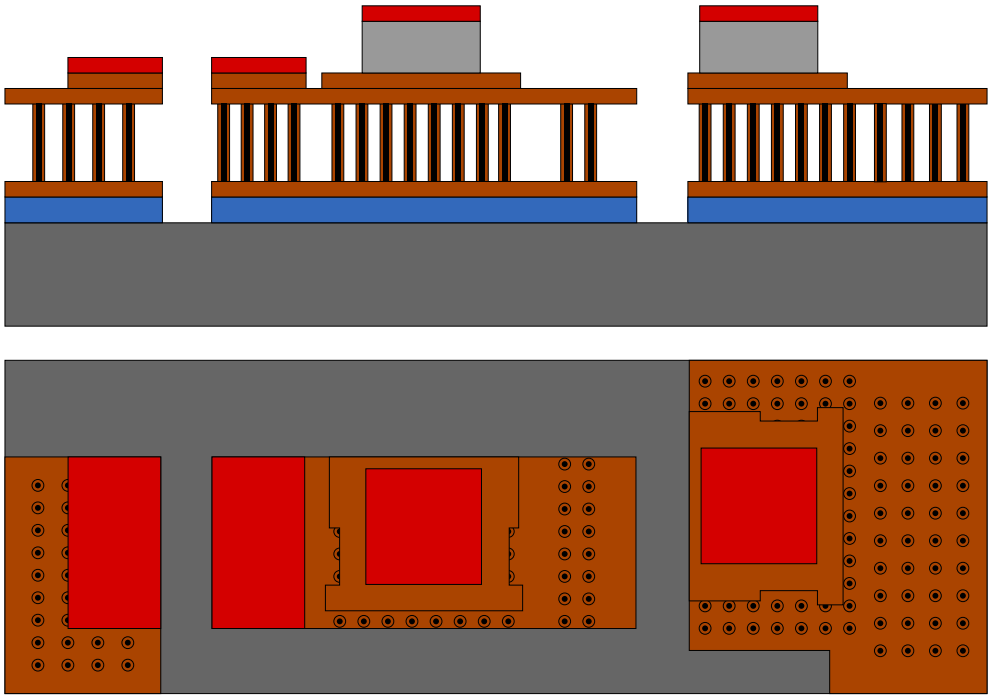

Figure 2.6.: Principal geometry of the simulation model with unfilled vias (top: side view, bottom: top view)

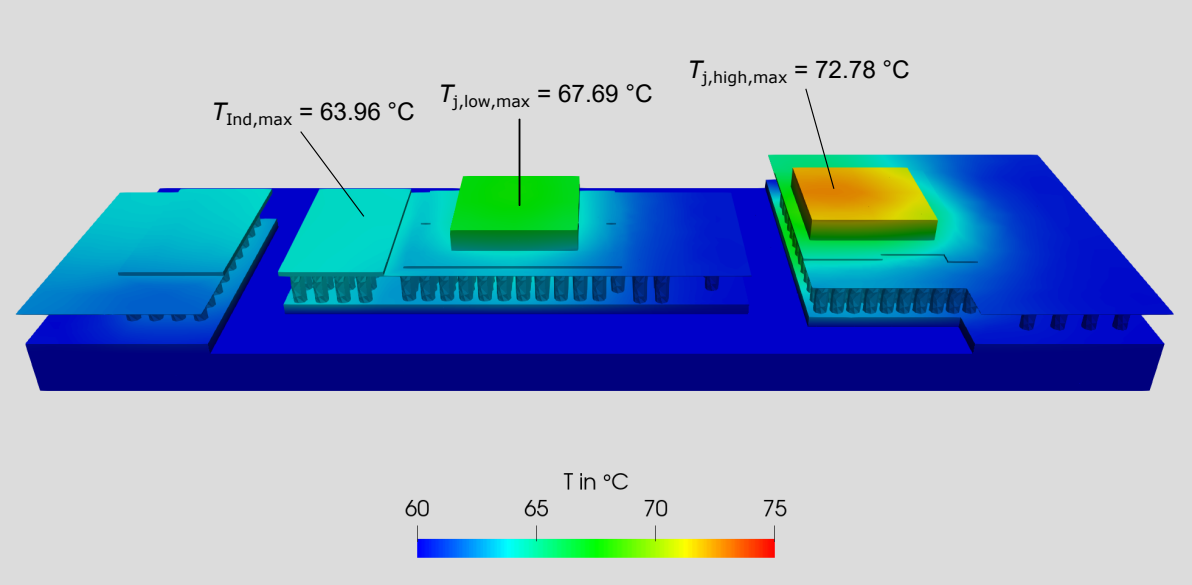

Figure 2.7.: Results of the thermal simulation with unfilled vias

The thermal conductivity of air $\lambda_{\text{air}} = 0.0262 \frac{\text{W}}{\text{mK}}$ [5] is small compared to copper so it does not really contribute to the heat conduction and, hence, the thermal resistance of the vias is increased due to the decreased copper cross section. The result is that the temperatures of all devices are higher than without modelling the holes as it can be seen in Figure 2.7. But the temperature differences of 0.08 °C on the inductor, 0.15 °C on the low-side and 0.27 °C on the high-side MOSFET are only very small. This means that the addition of the holes in the vias does not change the thermal behavior of the PCB significantly.

2.5. Simulation with Unfilled Vias and all PCB Layers

The last simulation configuration considers the thermal vias, their holes and additionally all PCB layers including the insulation layers like depicted in Figure 2.8 (insulation layers are green). The PCB has six copper layers and five insulation layers consisting of FR-4 material with a thermal conductivity of $\lambda_{\text{FR-4}} = 0.33 \frac{\text{W}}{\text{mK}}$ [6]. These layers contain the thermal vias that connect the copper contact of each device with the TIM thermally.

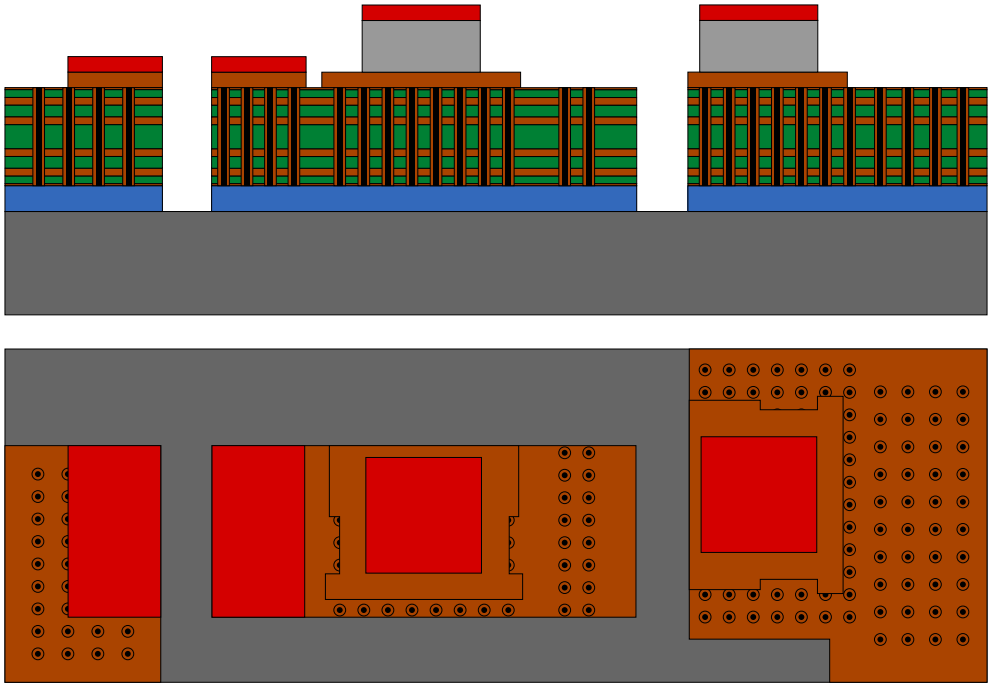

Figure 2.8.: Principal geometry of the simulation model with unfilled vias and all PCB layers (top: side view, bottom: top view)

Layer	Thickness
Top copper layer	35 µm
Insulation layer	135 µm
Copper layer	105 µm
Insulation layer	200 µm
Copper layer	105 µm
Insulation layer	390 µm
Copper layer	105 µm
Insulation layer	200 µm
Copper layer	105 µm
Insulation layer	135 µm
Bottom copper layer	35 µm

Table 2.2.: Structure of the PCB and thicknesses of the layers

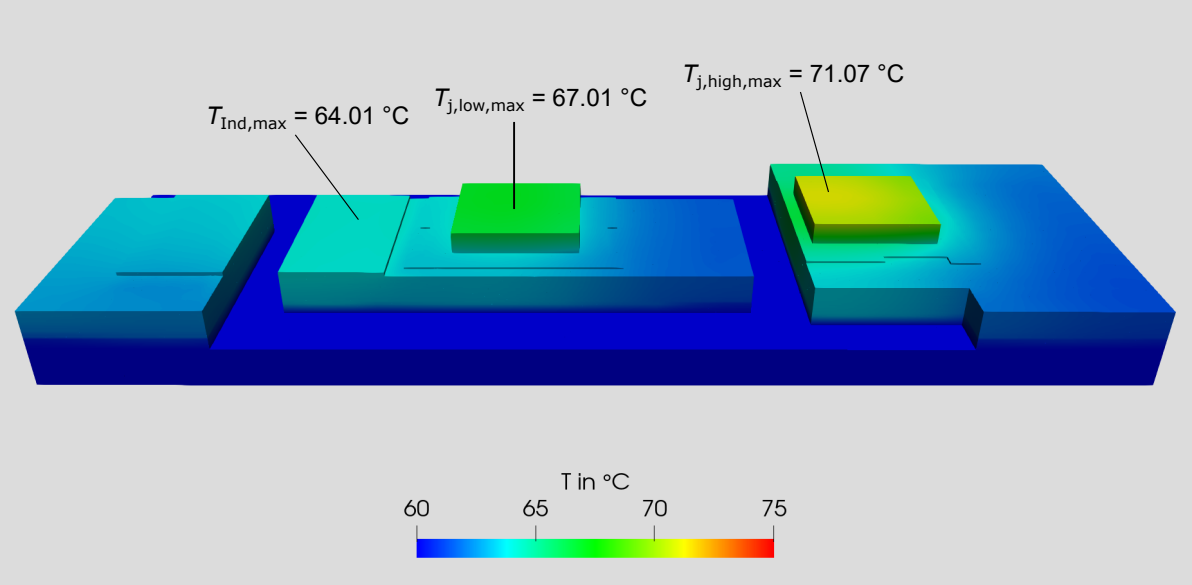

Figure 2.9.: Results of the thermal simulation with unfilled vias and all PCB layers

The structure of the PCB and the thicknesses of the layers are shown in Table 2.2. This geometry is the most complex one of all simulated ones regarding the generation of the geometry due to many overlapping 3D elements (see [4] for more details of geometry generation). This makes it complicated to assign each grid cell the correct material in *Sparselizard*. Besides, the computational effort is much higher because of many details that are small compared to the entire geometry. The mesh of this geometry consists of 4,971,712 grid cells with one refinement what is much more than with the other simulation models. This leads to a simulation time of $t_{\mathrm{sim}} = 21{,}056\,\mathrm{s} \approx 5.8\,\mathrm{h}$ what is about 40 times more than with the model that neglects the PCB layers.

Figure 2.9 shows that the maximum temperatures are smaller than with the simulation without the PCB layers. Like in the other simulations, the highest temperature of $T_{\mathrm{j,high,max}} = 71.07\,^{\circ}\mathrm{C}$ is in the high-side MOSFET and the second highest temperature of $T_{\mathrm{j,low,max}} = 67.01\,^{\circ}\mathrm{C}$ in the low-side one but both are far away from the critical junction temperature of $T_{\mathrm{j,max}} = 175\,^{\circ}\mathrm{C}$. As previously, the inductor is about $3\,^{\circ}\mathrm{C}$ cooler than the MOSFETs what is not critical.

2.6. Comparison of the Different Simulation Models and Future Improvements of the Simulation

In the previous sections a theoretical equivalent circuit diagram and four different simulation models are used to calculate the temperatures of the inductor and the two MOSFETs of a rail. The results of the maximum temperatures, the needed simulation time and the used number of grid cells of the simulation models is summarized in Table 2.3.

The easiest way to calculate the temperatures is the theoretical one since the computational effort is low and changes of parameters are easy to implement. But the disadvantage of this method is the assumption that the heat flows through the whole cross section of each element so it does not consider any 2D and 3D effects what makes the results unaccurate.

The first simulation model replaces the thermal vias by a box of homogeneous material with the same theoretical thermal resistance. In comparison to the theoretical model it considers 2D and 3D effects in the temperature calculation. This can also be seen in the results: Since the area of the vias replacing box is larger than the area of the copper contact, the heat does not flow through the whole cross section so the thermal resistance of the vias is larger than in the theoretical calculation. Hence, the temperature rise in the simulation is higher than in the theoretical calculation (see Table 2.3). For the high-side MOSFET the temperature difference between calculation and simulation of about 4 °C is the largest because the area of the box of the vias is the largest here and thus the relatively utilized cross section is the smallest. The number of grid cells and the simulation time is significantly smaller than with the other models.

In the second simulation model the thermal vias are implemented as solid cylinders of copper. This is more accurate from a geometric point of view but a bit more effort in generating this model and in computing the results is needed since about 13 times more grid cells and roughly 16 times more simulation time are needed (compare Table 2.3). The simulated temperatures with solid cylinders are slightly higher than with replaced vias. There is no exact explanation for these small differences since it is in the range of possible simulation errors. However, a possible reason for this could be that a part of

	Theoretical calculation	Replaced vias	Filled vias	Unfilled vias	All PCB layers and unfilled vias
$T_{\mathrm{Ind,max}}$	63.04 °C	63.70 °C	63.88 °C	63.96 °C	64.01 °C
$T_{\mathrm{j,low,max}}$	65.49 °C	67.13 °C	67.54 °C	67.69 °C	67.01 °C
$T_{\mathrm{j,high,max}}$	67.16 °C	71.87 °C	72.51 °C	72.78 °C	71.07 °C
t_{sim}	-	18 s	286 s	504 s	21,056 s ≈ 5.8 h
n_{cells}	-	22,936	305,328	562,136	4,971,712

Table 2.3.: Maximum temperatures of the inductor, the low-side and high-side MOSFET calculated theoretically and with different simulation models, simulation time (without meshing) and number of grid cells of the simulation models

the thermally well conducting vias is farer away from the loss producing devices which do only hardly contribute to the heat flow. This would also explain why the high-side MOSFET shows the highest temperature difference because here are many vias not directly below the copper contact of the transistor (see Figure 2.4).

The next improvement is the addition of the holes in the thermal vias in the simulation model. The creation of the geometry is only a bit more complicated and the computational effort just a bit higher due to about 84 % more grid cells but the real PCB is mapped much better with this geometry. Furthermore, less than twice the simulation time is needed when considering the holes. Compared to the results with copper filled vias the temperatures are increased a little bit because the holes that consist of air are bad thermal conductors and, hence, the thermal resistance is higher.

In the last simulation geometry, all PCB layers are added which is the model that is closest to the real PCB. Due to its details it is the more complicated to build up this geometry in *Sparselizard* and it is a much larger computational burden. In contrast to the other simulation models, the number of grid cells and the simulation time are notably increased what makes this model uncomfortable to simulate. The thermal conductivity of the insulation layers is not that high but it still represents an additional heat conduction path besides the thermal vias. That is why the temperatures simulated with this model are lower than without PCB layers except the inductor temperature which is increased by 0.05 °C. This very small difference could possibly be an error of mapping the small details.

As a conclusion it must be noted that the simulated temperatures in Table 2.3 do not differ that much from each other because the thermal resistances of the TIMs dominate the thermal behavior (see Table 2.1). Furthermore, the TIMs are far below the heat sources (below the PCB) so the cross section is highly utilized and the thermal resistances are hardly reduced by 2D and 3D effects. That is why a detailed modelling of the thermal vias is not necessary and a model where boxes replace the vias is good enough to obtain sufficiently accurate results what saves time during simulation. For an estimation of the temperatures a theoretical calculation with a thermal equivalent circuit diagram like in Figure 2.1 is recommended because it is simple to calculate and to vary parameters.

All in all, the calculation and the simulations show that there is a large safety margin to the critical junction temperature of 175 °C of the MOSFETs and the temperature rise of the inductor is only about 3 to 4 °C compared to the ambient temperature. As a consequence, the thermal design of the PCB is fine but there is still some space for improvements of the thermal design of the PCB for example by reducing the size of the MOSFETs.

For future simulations the accuracy can be increased by building a model where the PCB layers are not limited to the three paths like in Figure 2.8 but where the layers are connected beyond the surfaces of the TIMs so the electronic devices are thermally coupled. Another improvement is to model the inductor as one box producing the losses instead of two because the assumption that the heat flows half through the left and half through the right inductor contact does not need to hold in reality.

3. Inductor Simulation

The magnetic topology was developed which involved a coupled inductor without the back conductor. The two coils are connected in parallel essentially reducing the inductor resistance. As it would be seen later the topology has an advantage of reducing the DC ohmic loss and hence the copper losses. FEM simulation was carried out in the previous semester, to optimize the geometry of the inductor by minimizing the total losses. Another cost function used for the optimization was to avoid the magnetic saturation. The entire design procedure used by the previous semester group, is explained in detail in [1]. An error was found later in considering the coupling factor between the two windings of the inductor, due to which the optimized inductor was over-dimensioned. The magnetic topology was reevaluated further and was corrected in the end. But further optimization with the corrected topology could not be done due to time constraint.

Aim of this simulation is to optimize the new inductor topology and to minimize the required post-processing in the process of FEM-simulation. The reduced post processing results in lesser effort and possibility to easily automate the simulation process. To minimize the required post-processing, transient simulation was implemented and tested for its validity. Hence, two separate AC and DC simulation could be eliminated by using transient analysis for inductor simulation.

3.1. Optimization

Optimization of the improved topology was done using Ansys-Optimetrics at first, with the cost-function $L \geq 10\,\mu\text{H}$, by varying leg height and length of air gap. The result is

summarized in the given Table 3.1

Inductance	Geometry	$P_{\Omega DC}$	$P_{\Omega AC}$	P_{Core}	P_{Total}
10.1 µH	Turns = 9, air gap = 0.52 mm leg height = 24.44 mm width of winding = 13 mm	1.67 W	0.3967 W	0.0459 W	2.1126 W

Table 3.1.: Results from Optimetrics analysis on Ansys

The simulation did converge but only inductance was optimized using this method. The core and copper losses would have to be optimized separately, that is a slower convergence process, and hence was not implemented further. In order to minimize the post-processing required during simulation, transient simulation was implemented. Another advantage of using the transient solver is, the ability to define the exact triangular current distribution with the exact duty cycle, resulting in analysis of inductor behaviour in time domain. The transient analysis would give insights on the variations of losses with respect to time. Also the transient analysis simulation process is much less cumbersome compared to separate AC and DC analysis used in the previous semester.

3.2. Core Loss Calculation

The excitation current is non-sinusoidal which generates non-sinusoidal magnetic flux density $\hat{B}$ waveform and hence the core loss due to the excitation current depends on the slope of the current, its duty cycle (D), core volume (V_{Core}) and the total time of a single period (T). For core loss calculation improved Steinmetz equation should be used as in Equation 3.1 [3]. Due to DC component in the current the hysteresis loss calculated must include the effect of the minor loop of hysteresis curve with DC offset. This can be modeled using ferrite material definition parameter k_{DC} on Ansys-Maxwell. k_{DC} would be automatically calculated during the simulation process. There is a possibility of calculating this coefficient manually. Detailed information can be found in [7]. The Steinmetz parameters α and β are estimated using the data sheet curves of power vs

magnetic flux density at different frequencies f.

$$P_{\mathrm{C,IGSE}} = \frac{V_{\mathrm{Core}} C_{\mathrm{i}} (\Delta B)^{\beta-\alpha}}{T} \cdot \left[DT \left(\frac{\Delta B}{DT} \right)^{\alpha} + (1-D)T \left(\frac{\Delta B}{T-DT} \right)^{\alpha} \right] \tag{3.1}$$

with

$$C_{\mathrm{i}} = \frac{C}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} \, \mathrm{d}\theta} \tag{3.2}$$

Transient analysis is a time domain approach and the instantaneous core loss calculation in the time domain is challenging especially the calculation of hysteresis loss. Ansys solver uses similar $\frac{\mathrm{d}B}{\mathrm{d}t}$ approach as given in Equation 3.1 for calculating the core losses of the inductor [8], where $\theta = 2\pi f t$, (f:frequency of the excitation current).The irreversible component of magnetic field strength H_{irr} is associated with hysteresis loss. The instantaneous hysteresis loss can be calculated using Equation 3.3. Calculation of H_{irr} is important for accurate prediction of hyteresis loss. A through explanation regarding this topic can be found in [8].

$$\begin{aligned} p_{\mathrm{h}}(t) &= H_{\mathrm{irr}} \cdot \left(\frac{\mathrm{d}B}{\mathrm{d}t} \right) \\ H_{\mathrm{irr}} &= \frac{1}{\pi} \cdot k_{\mathrm{h}} \cdot B_{\mathrm{m}} \cdot \cos\theta \\ k_{\mathrm{h}} &= \frac{(k_1 - k_{\mathrm{c}} \cdot f_0^2)}{f_0} \end{aligned} \tag{3.3}$$

Similarly the eddy current loss is given by Equation 3.4. The classical eddy current loss component can be represented using k_{c}. ρ is the conductivity of the ferrite material used and d is the thickness of the lamination.

$$\begin{aligned} p_{\mathrm{c}}(t) &= \frac{1}{2\pi^2} \cdot k_{\mathrm{c}} \cdot \left(\frac{\mathrm{d}B}{\mathrm{d}t} \right)^2 \\ k_{\mathrm{c}} &= \pi^2 \cdot \rho \cdot \frac{d^2}{6} \end{aligned} \tag{3.4}$$

The excess loss in the inductor is calculated using Equation 3.5. The coefficient k_{e}

can be given by $k_e = \frac{k_2}{f_0^{1.5}}$. The coefficients k_1 and k_2 are determined using the loss curve provided by the manufacturer in the data-sheet. f_0 being the frequency at which the loss curve is measured.

$$p_e(t) = \frac{1}{C_e} \cdot k_e \cdot \left|\frac{dB}{dt}\right|^{1.5}$$
$$C_e = (2\pi)^{1.5} \cdot \frac{2}{\pi} \cdot \int_0^{\pi/2} \cos\theta^{1.5} d\theta \tag{3.5}$$

Ansys calculates the core loss based on this dynamic core loss model in time domain. It can predict the instantaneous hysteresis loss with a good accuracy using the parameters and coefficients used in the frequency domain. The instantaneous core loss plot of the given inductor topology is seen in the Figure 3.1. The core loss depends on $\left(\frac{dB}{dt}\right)^{\alpha}$ as seen from the Equation 3.1. The Steinmetz coefficient α was estimated to be 1.5. During the rising edge of the current slope, the losses are smaller than during the falling edge of the current slope. This is true since $P_{\text{Core}} \propto \left(\frac{dB}{dt}\right)^{1.5}$, and the slope of rising edge is

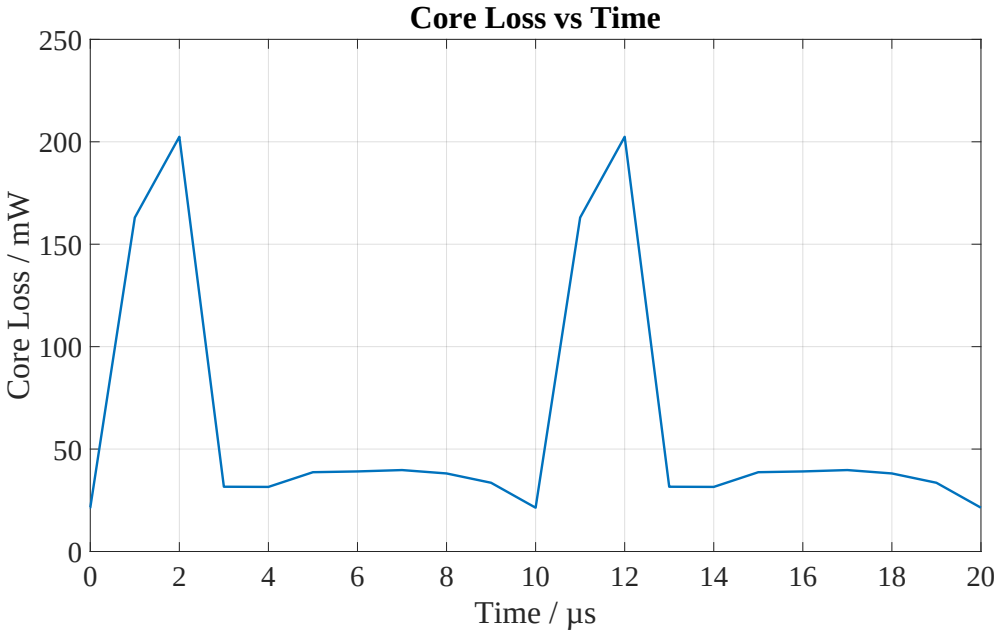

Figure 3.1.: Transient simulation: Core loss vs Time

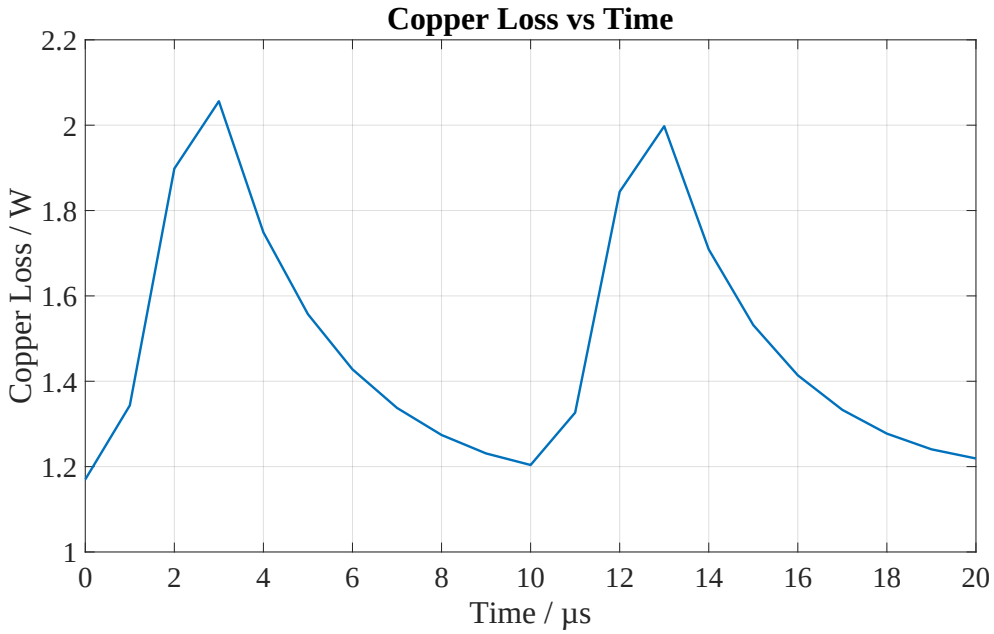

Figure 3.2.: Transient simulation: Copper loss vs Time

greater than the slope of falling edge of current. Therefore on comparing the simulation results with the formula in Equation 3.1, the estimated losses on Ansys is verified. The copper loss vs time plot can be seen in Figure 3.2. Due to eddy current effect and other no-linear effects in the winding, the copper losses waveform is not only proportional to the excitation current.

3.3. Simulation Procedure Transient Analysis

The excitation current is given in Figure 3.3. The general simulation workflow is represented in Figure 3.4. Three cycles of current is simulated since optimum and correct results are obtained when the simulation is continued for two cycles or more. Three cycles are sufficient taking into consideration the duration for a single parametric variation.
The process of transient analysis is summarised below:

- Select the solution type using Tab Maxwell 3D → Solution Type → Magnetic

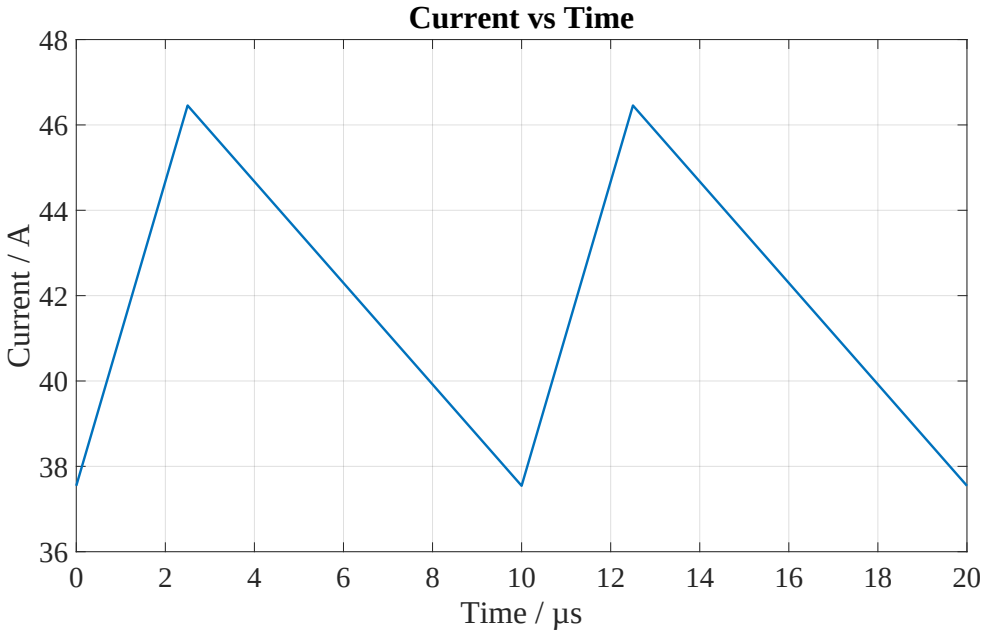

Figure 3.3.: Excitation current in the Simulation.

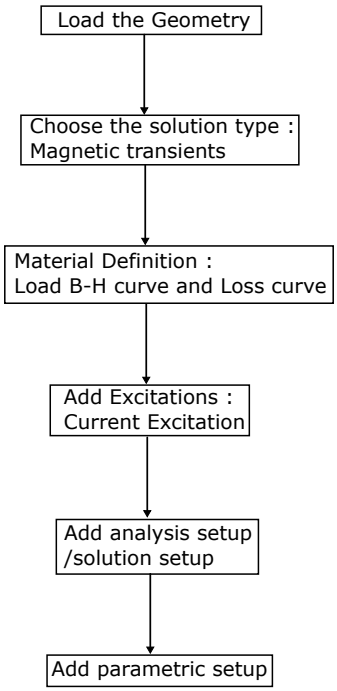

Figure 3.4.: General simulation workflow on Ansys-Electronics Desktop

Transient.

- Material definition by importing the B-H curve and core loss vs B field at various frequency. To calculate the core loss and eddy effect, the core loss and eddy effect needs to be activated by Maxwell 3D → Excitation → Set eddy effect (Select the Winding) and Set Core loss (Select the core geometries).

- To assign current excitation on winding geometry select the 2D geometry then Maxwell 3D → Excitation → Add Winding. For the defined winding pwl_ periodic (ds1,time) command is used to manually input the data points to get the desired current waveform or import the required waveform in *.tab* format. Assign coil terminal to the winding added to the design using Maxwell 3D → Excitation → Assign → Coil Terminal.

- Add solution setup using, Maxwell 3D → Analysis setup → Add solution setup.

- To add parametric setup, Maxwell 3D → Optimetrics analysis → Add Parametric. Here sweep definition needs to be defined including all the parameter variations. The leg height was varied from 20 mm to 30 mm, the air gap was varied from 0.4 mm to 0.6 mm and width of winding was varied from 11 mm to 13 mm.

3.4. Simulation Results

Transient analysis is chosen for parametric analysis in this semester. The configuration with lowest overall loss is given in Table 3.2. The advantage of this configuration is the lower height of the core which could be advantageous for milling the core without much wastage of ferrite material and can reduce the housing height.

The losses of other configurations are represented in the bar chart in Figure 3.5 taking eddy effect into consideration in the winding. Most of these configurations are operating lower or close to the saturation flux density B as indicated by dashed line on Figure 3.5. The labels for Figure 3.5 are described in Appendix A.1 Table A.1.

Version	Inductance	Geometry	P_Ω	P_{Core}	P_{Total}
New	7.9505 µH	Turns = 9 leg height = 22.24 mm width of winding = 13 mm	1.55 W	0.037 99 W	1.6 W
Old	9.8 µH	Turns = 8 leg height = 25 mm width of winding = 11 mm	2.01 W	0.044 W	2.05 W

Table 3.2.: Configuration with lowest total loss as given in Figure 3.6

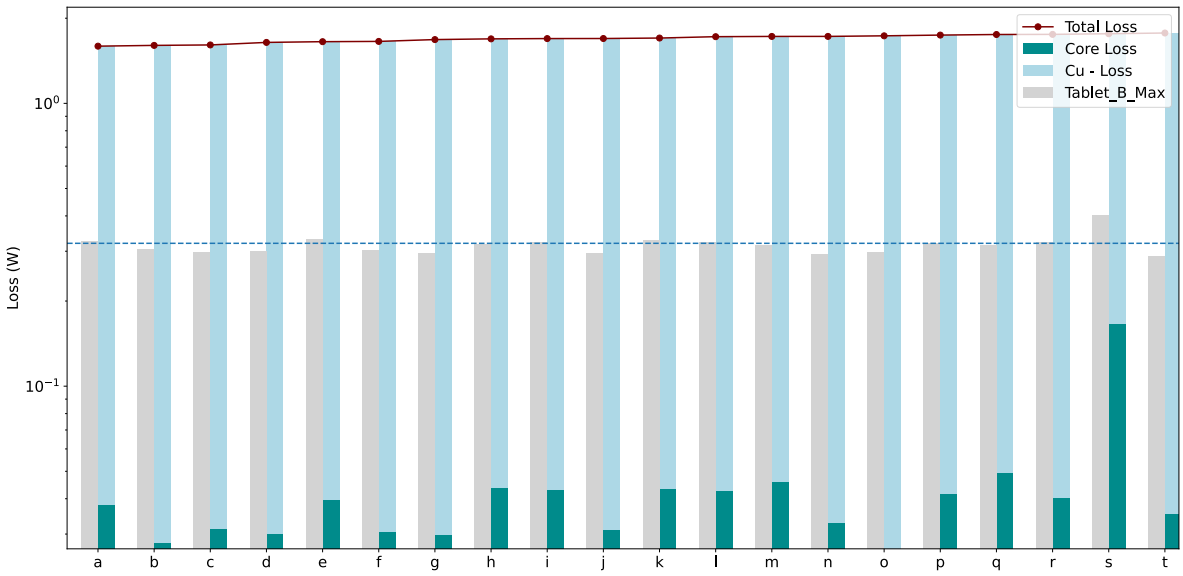

Figure 3.5.: Losses and B_{max} vs parametric variations (logarithmic scale)

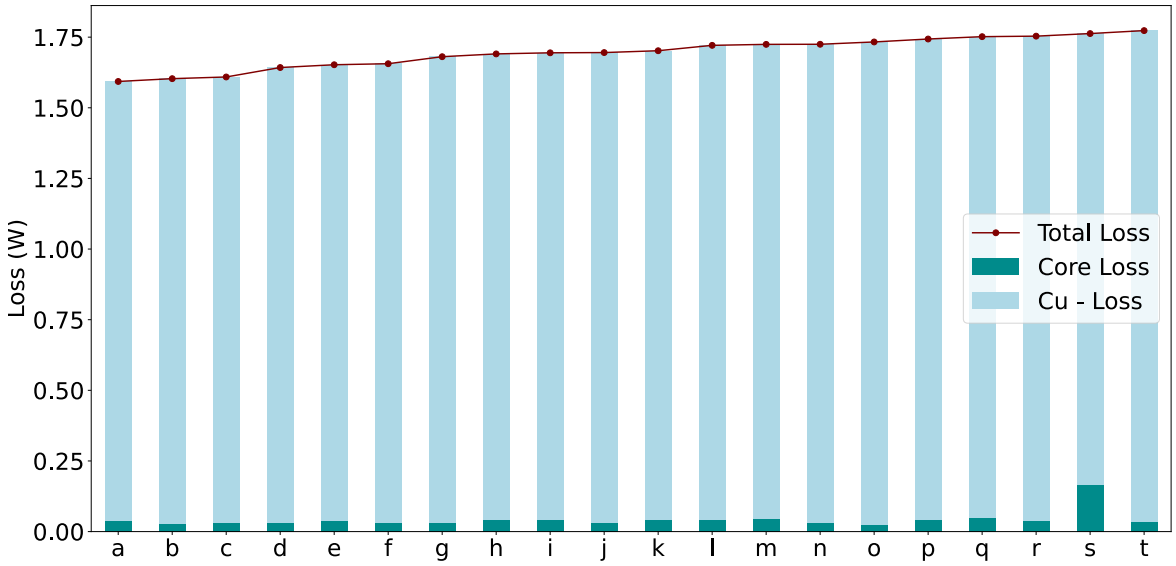

Figure 3.6.: Losses vs parametric variations

Out of the total losses core losses are the lowest due to the fact that all the configurations are operating below saturation and lower ripple so losses are due to small minor hysteresis loop. This can be clearly seen in Figure 3.6. The copper loss is much greater than the core losses and hence the winding with lowest copper loss comes out to be the configuration with lowest total losses. The configuration with the lowest losses mentioned in Table 3.2 also operates around the decided saturation point.

The AC and DC copper loss contribution to the total loss is represented in Figure 3.7. There exists a configuration that shows very high AC ohmic loss component due to non-linear effects in the winding due to eddy effects. The labels for Figure 3.7 are described in Appendix A.1 Table A.2.

3.5. Conclusion

The optimization using transient analysis resulted in lower post processing. Various configurations were analysed for comparison. The resultant configuration was chosen considering the configuration with lowest losses and lower core volume. The losses were

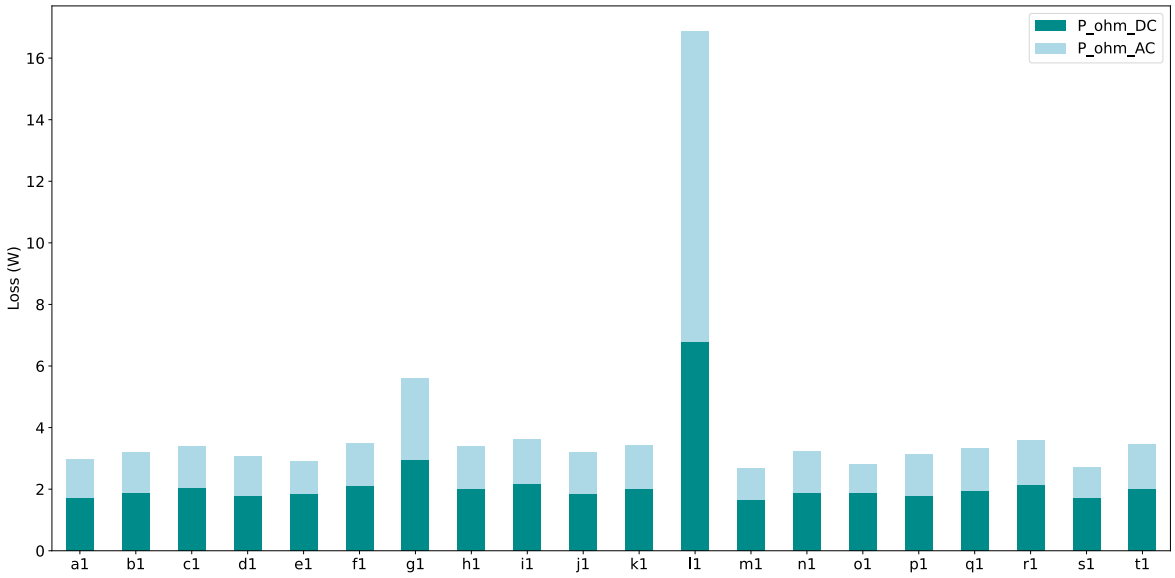

Figure 3.7.: AC and DC ohmic loss content in the total ohmic loss in various configurations of the inductor topology

reduced by 22 % and volume of the ferrite is reduced by 31 %, which can be seen in Table 3.2. The copper losses dominates the overall losses in the inductor. The core losses are low since the inductors are operation below saturation flux density B and lower ripple. To sum up the core losses were lower owing to a smaller minor loop of hysteresis curve formed due to larger DC content of the current than the AC content and lower ripple in the flux.

4. Housing

Because the DC/DC converter is specified for automotive application, an appropriate housing is needed, that also provides a path for the liquid cooling. Although the housing design is theoretical, it is possible to compare the results with the previous converter versions. The hole design was made with the 3D-CAD-Program SolidWorks.

4.1. Requirements

When designing a housing for automotive applications numerous conditions must be fulfilled, which can vary from special requirements made by the client to international safety standards. Furthermore, the design should be compact and lightweight while the used components and materials are cheap and easy to produce. Finally, the physical connections, for example to other devices, to the bus network or the cooling system, should be realized by connectors that are already used in automotive applications and thus provide a good compatibility. While taking the conditions from above into account, some relaxations are made for the housing of the 2 kW converter (V11.0). From the international safety standards only ISO 20653 will be considered, which describes the protection of electrical equipment against foreign objects, water and access [9]. Other important standards like ISO 16750-3, that define the mechanical stresses to electronic devices in road vehicles [10] will receive no consideration during this semester. Also, the material for the housing just includes aluminum and plastic, because only this material can be processed in the lab for a future prototype.

4.2. Design of the Housing

The main target of the housing is, beside the protection of the circuit, the cooling of its components. As described above, the most important parts to be cooled are the MOSFETs. Differing from the previous housing concepts the inductors do not have to be cooled. Therefore, one aluminum plate is designed which will include a path for the liquid of the cooling system. First, the structure as shown in Figure 4.1 will be milled into the material. Afterwards holes will be drilled according to the red arrows. The resulting holes will be sealed by welding the aluminum in the area so just the in- and outlet remains open. The top side of the bottom plate Figure 4.2 includes some pedestals, that will provide a thermal connection between the thermal vias of the PCB. For the TIM space is also included.

The next step in the design process was the selection of the connectors. For the 11th. version of the converter a 12 V, 48 V and Ground connection is provided. For the liquid cooling system, a fitting [11] is selected (Figure 4.3) that meets the SAEJ2044 standard for road vehicles [12]. On the electric side a 3 position connector is chosen (Figure 4.4) which is also designed for automotive usage [13] that fulfills the degree of protection IP6K9K from ISO 20653. Also of interest is the maximum current rating of the connector with is 200 A. This is above the maximum current of the 2 kW converter with 166.67 A at the 12 V port. While the fittings of the cooling system could be mounted directly to the bottom part, for the electrical connector a separate aluminum plate is designed. This plate must withstand potential mechanical stresses from the connector, so a plastic material was not chosen here. The complete housing can be seen in Figure 4.5 were the two described aluminum parts are screwed together. The remaining part of the housing is covered with a plastic case, which follows the contour of the converter to reduce the volume. In Figure 4.6 the inside of the housing is shown. Here, the copper blocks are visible, which link the PCB to the connector.

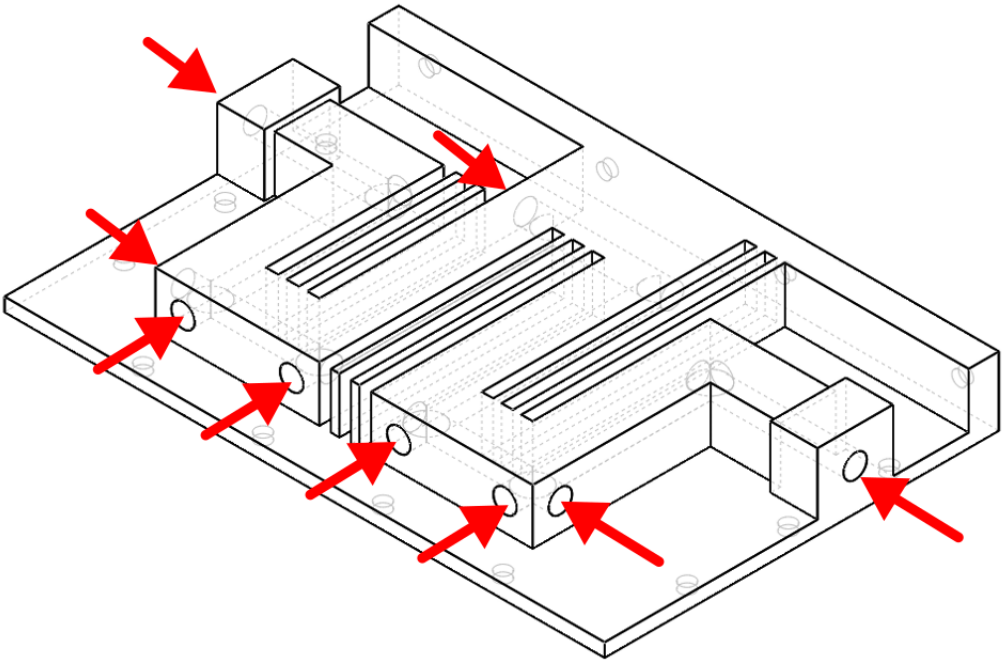

Figure 4.1.: Bottom of the housing with the liquid path. The red arrows show the drilling holes

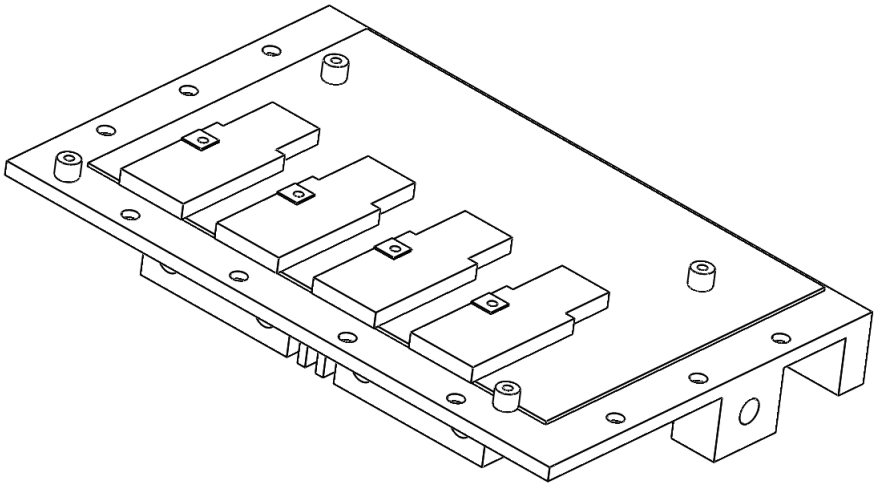

Figure 4.2.: Top of the bottom part with the pedestals for the thermal connection between housing and PCB

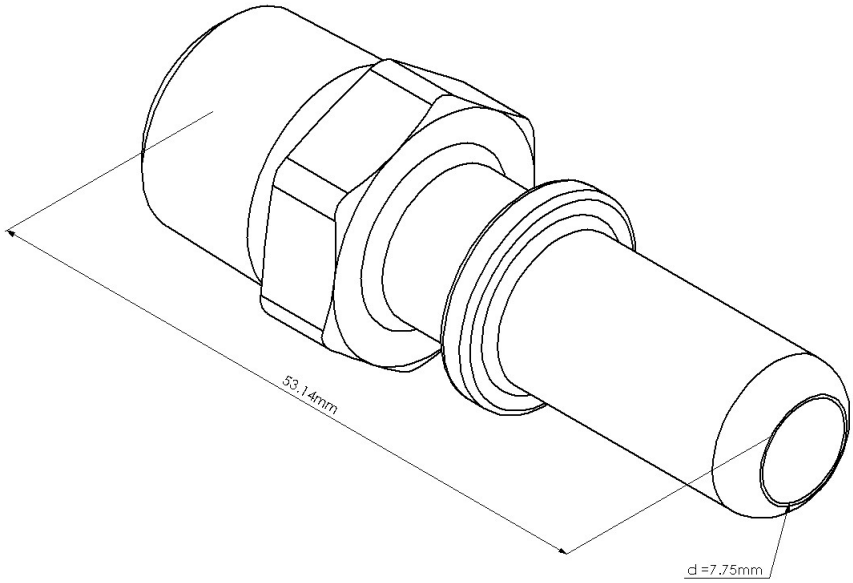

Figure 4.3.: SAE J2044 fitting from Parker [11]

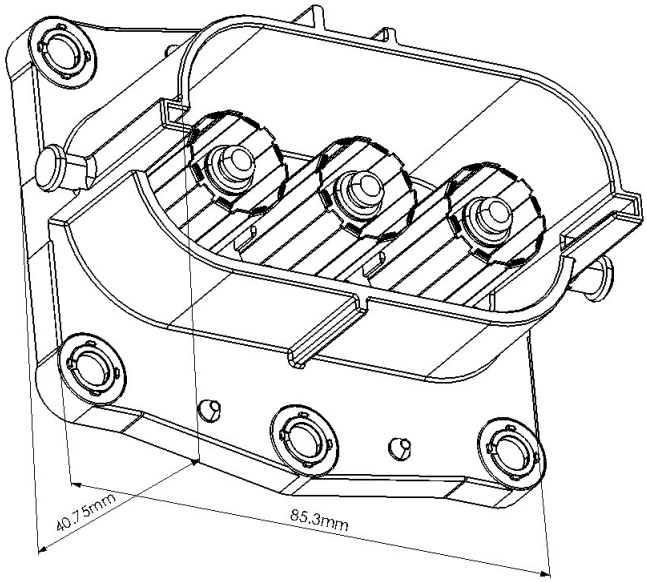

Figure 4.4.: AMP+HVP800 connector from TE [13]

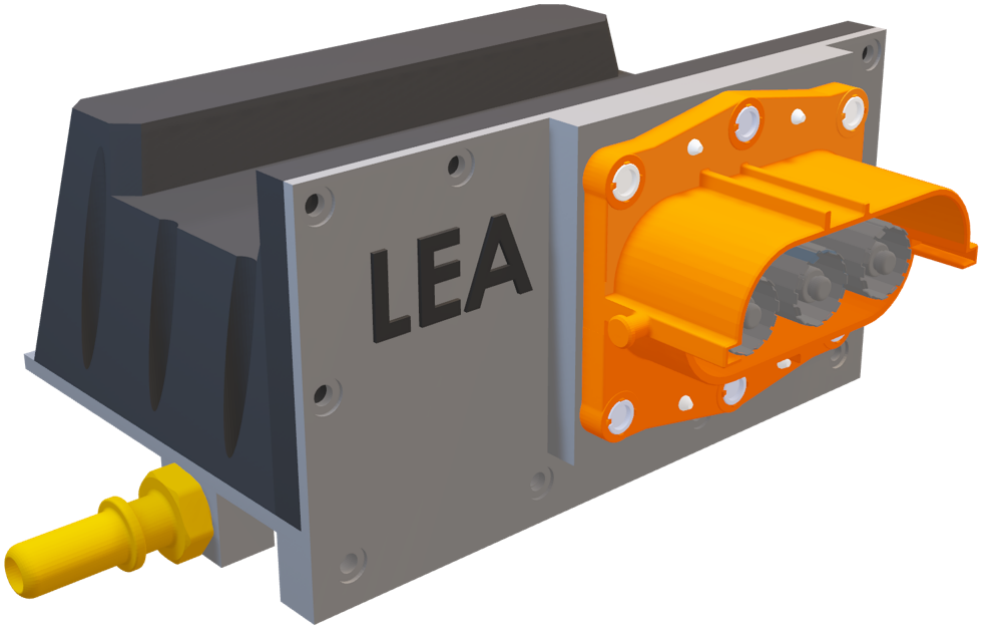

Figure 4.5.: Outside the housing

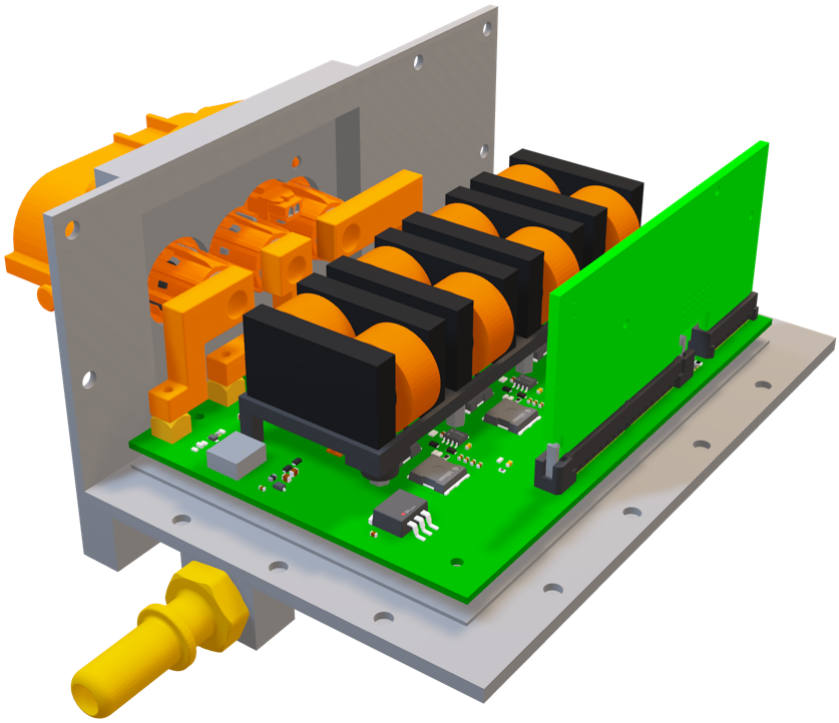

Figure 4.6.: Inside the housing

4.3. Conclusion

The housing of the 2 kW converter was designed with a liquid cooling opportunity. Unfortunately a liquid cooling system is not given in the lab, therefore the housing could not be tested. But it is possible to compare the new housing concept with the designs of the previous 1 kW converter versions. This is done in Table 4.1 by listing the power densities. A direct comparison between the V10.0 and V11.0 housing results in a reduction of the power density by 33 %.

Converter Version	V11.0 (2 kW)	V10.0 (1 kW)	V9.0 (1 kW)
Power density in $\frac{\text{kW}}{\text{dm}^3}$	1.10	1.64	1.37
Volume in dm^3	1.81	0.61	0.73

Table 4.1.: Comparison of power density and volume of the different converters

Three major reasons can be named that explain this result. First, the MOSFETs that are used in this version are of Si while the previous Converters used GaN MOSFETs [1]. Because of the lower power density and the lower switching frequency of the Si MOSFETs, the PCB size increased. The second reason could be found in the increased size of the electrical automotive licensed connector, in previous designs a bushing was used instead. Eventually the most important reason is found in the multiple (10) iterations the 1 kW Converters went through in the last semesters. This is the first time a 2 kW converter is build up and improvements will lead to a smaller volume in the future. The biggest improvement could be made by changing the position of the control card. As well it would be possible to abandon a separate control card from the converter and implement the microcontroller to the PCB of the converter.

5. Inductor Build-Up

This chapter will cover the basic steps of the building process of the inductors as well as some measurements of the finished one. Based on these results some improvements of the design could be found and utilized. There, basic production will be explained to enable following groups tracking issues that could arise during operation of the 2 kW converter. Also, it was the first time inductors of the DC/DC converter project were built with the CNC-Milling machine in the lab so this part of the report could be used as a instruction by upcoming projects.

5.1. Design of the Footprint

While the previous group was focused on an optimal design of the inductor with respect to the losses, saturation and a compact geometry [1], no electrical connection between the PCB and the winding of the inductor was described yet. Hence, the task of this semester group is to find a connection which fulfils the following requirements:

- fit into the compact inductor design
- provides eight full turns
- small footprint on the PCB

The process of finding the best connection could be described as follows. First the CAD model of the inductor was used to get a possible way to add the connection in theory. Here the dimensions of the ferrite, copper and air gaps could be viewed in detail. To

verify that this connection could be realised, a practical setup is used. Because the ferrite parts of the inductor are not available at this point of time a 3D-Print of the inductors cuboid and cylinder is used (see Figure 5.1). In the second step the copper is cut out and wind up according to the results of the first step. If the design of the connector does not fit with the geometry of the inductor for example because of the stiffness of the copper or the height of the solder material, step one must be repeated. The process took two iterations before the final connection between the inductor and the PCB as shown in Figure 5.2 was found.

5.2. Basic Production Steps

The elementary parts of the inductor are the winding, the ferrite and the air gap material, see Figure 5.3. There basic production will be explained in the following.

5.2.1. Winding

The two windings of every inductor are cut out of a 0.5 mm copper sheet in form of an "L" and one side is isolated with 0.05 mm of Kapton tape. To bring the copper into a shape of a spiral one side is fixed in a vice while the other side is connected to an electric screwdriver. Two windings are connected afterwards by soldering them together.

Figure 5.1.: 3D-Print from the cuboid and cylinder as a model of the ferrite parts

Figure 5.2.: Model of the inductor with connection to the PCB (footprint)

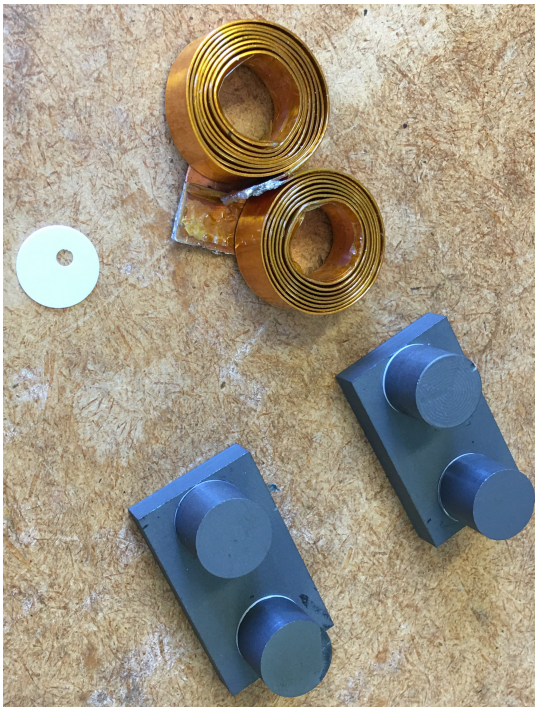

Figure 5.3.: The basic inductor components: winding, air gap material and ferrite core

Because the parasitic capacitance of the inductors should be small, the layers of copper must be as tight as possible. This results in mechanical stress in the corners of the "L" and can cause the copper to break like in Figure 5.4.

5.2.2. Ferrite

The special design of the ferrite would be difficult to build by hand and thankfully a CNC-milling machine which can work on ferrite is available in the lab [14]. For the process of milling a CAD-Modell of the desired parts is needed along with an object of ferrite material from where the parts are milled out. From this object a CAD-Modell is also needed to find out the best position where to cut out the parts. As can be seen in Figure 5.3 the inductor consists of two cylinders and two cuboids with a simple shape [1]. The dimension of the cylinder: $r = 7.36\,\text{mm}$ and $h = 12\,\text{mm}$. From the cuboid: $a = 6.81\,\text{mm}$; $b = 43\,\text{mm}$; $c = 12\,\text{mm}$.

Because the design of the inductors was made with the ferrite material N95 from TDK [15] it was decided to use a U-Core [16] of this material from where the parts could be milled out. Although the yield of this geometry is low, no other object of N95 was available that would allow to cut out the parts of the inductor. The arrangement for the milling of the cuboid parts is shown in Figure 5.5.

Unfortunately, the dimensions of the milling head do not allow to cut out two rows of cuboids in the U-Core, therefore just 16.6 % of the material can be used in this case. Even though enough U-Cores were ordered, just four cylinders and four cuboids were milled because of damages during the milling process. According to the laboratory staff the reason was the huge amount of wasted material that led to a fast wear of the milling head. As a result, the head could break the brittle material. Also, it should not be hidden, that one core broke during transportation. Consequently, it was searched for an alternative object that will increase the yield of the milling. But no object of N95 could be found, as mentioned above. Finally, it was decided to use ferrite blocks of Fi395 material from Sumida [17] which were left from the research project HELENE. In Figure 5.6 the arrangement of the cuboids is shown in one of these blocks. The yield

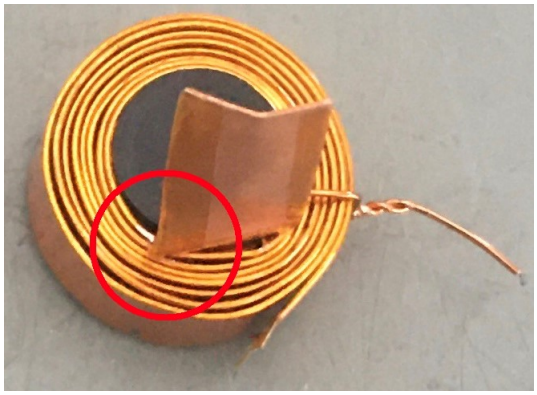

Figure 5.4.: Broken copper on the marked area due to mechanical stress during the winding process

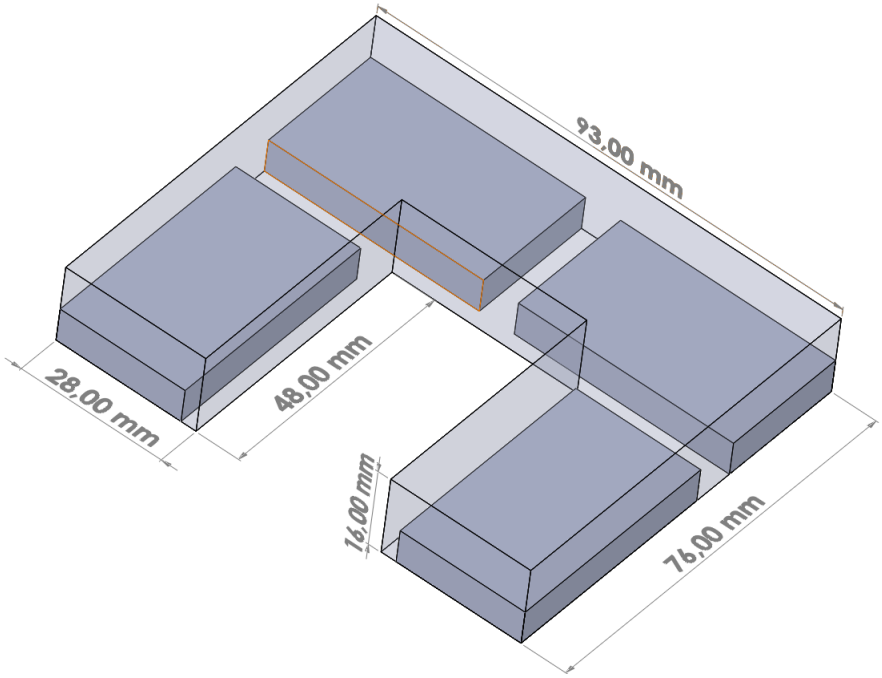

Figure 5.5.: Arrangement in the U-Core

of this block has a value of 26 %. Because the ferrite material is produced by another manufacturer the difference of the most important material parameters are compared in Table 5.1. The differences are small and the impact on the simulated inductance value or losses could be neglected. Thus, both materials will be treated as same in this project.

	N95	Fi395
Initial permeability μ_i	3000	2300
Flux density (H = 120 A/m)	525 mT (at 25 °C) 410 mT (at 100 °C)	530 mT (at 25 °C) 370 mT (at 100 °C)
Relative core losses	425 $\frac{kW}{cm^3}$ (at 25 °C; 100 kHz; 200 mT) 350 $\frac{kW}{cm^3}$ (at 100 °C; 100 kHz; 200 mT)	420 $\frac{kW}{cm^3}$ (at 25 °C; 100 kHz; 200 mT) 340 $\frac{kW}{cm^3}$ (at 100 °C; 100 kHz; 200 mT)

Table 5.1.: Comparison of the different ferrite materials Fi395 [17] and N95 [15]

5.2.3. Air Gap

The air gap must have a total distance of 2.16 mm and is equally distributed to the contact area between the cylinder and cuboid as shown in Figure 5.7. To enable the distance of 0.54 mm an Aluminium Oxide Ceramic plate originally designed for a TO-Case of a semiconductor is used as in Figure 5.8. The Ceramic is normally used as an electrical isolator, that has a low thermal resistance. Although the thermal properties allow the cylindric part of inductor to be dissipate heat to the cuboid part and thus to the ambient the low losses of the inductor do not make this necessary. More important is the possibility of the ceramic to be milled in the CNC-Machine and therefore a small variation in the air gap is possible. After milling the ceramic, it must be combined with the ferrite parts which is done with thermal resistant two-part epoxy (glue) that is usable for ferrite and already used in the laboratory [18]. A test was made to find out the distance that is added by the glue to the air gap. The glue increased the air gap by 0.01 mm on every glued surface. This means the total air gap of the inductor has a value of 2.2 mm which is 1.9 % more than originally calculated. Finally, the winding and core of the inductor are combined and the copper for the footprint is added. In Figure 5.9

one cuboid must be added before completing the inductor.

5.2.4. Measurement

After finishing three inductors, they were analysed with a spectrometer [19] for their inductance and resistance form 100 Hz to 1 MHz. The results of all three inductors look the same but showed a value of lower inductance than expected Figure 5.10 where the dashed line marks the inductance of 8 µH predicted by the simulation from the previous group [1]. This difference could be caused by either a wrong assembly of the inductors or an incorrect simulation. The use of different ferrite material (Fi395 instead of N95) can be eliminated as a reason because one of the three inductors was built with N95.

Because some effort was put into a precise build-up of the inductor the reason could lay in the simulation, although no error was found here that could explain the measured value. As a result, it is most likely that idealized assumptions of the simulated inductor model led to the differences.

To solve the problem, it was decided to reduce the air gap and thus increase the inductance value. This was done in Figure 5.11 where two ceramic plates are removed and two layers of are Kapton are placed. To enable a connection for the glue, a hole is cut into the tape. Before gluing the parts, the inductance was measured with the impedance analyser. For the measurement the parts are pressed together by hand and showed an inductance value of 7.81 µH at 100 kHz. After combining the parts with the two-component epoxy the measurement was repeated and showed a value of 7.33 µH at 100 kHz Figure 5.10. An explanation for this could be the wider air gap because of the glue material or the high pressure while holding the parts in hand. This behaviour must be considered in the future and the two Kapton layers should be removed to meet the value of 8 µH. The final inductor is shown in Figure 5.12.

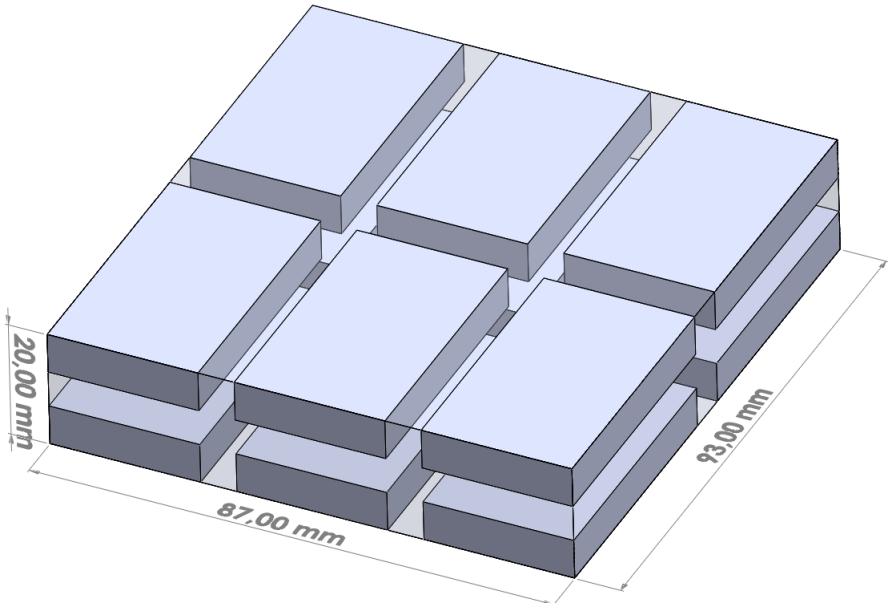

Figure 5.6.: Arrangement in the cuboid from HELENE

Figure 5.7.: The white air gap material is visible at the surface between the cuboid and the cylinder

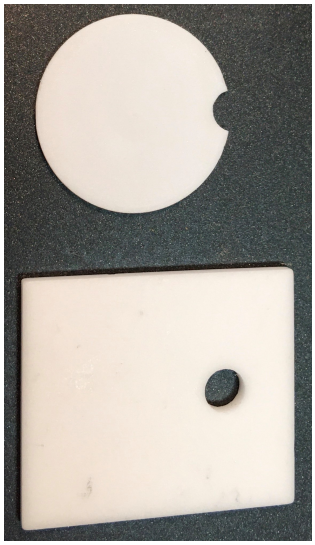

Figure 5.8.: The Aluminium Oxide Ceramic plate for the TO-case before and after the milling process

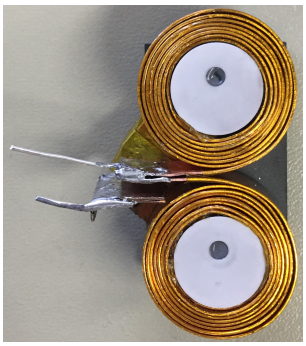

Figure 5.9.: A nearly finished inductor with attached ceramics. One ferrite cuboid must be added

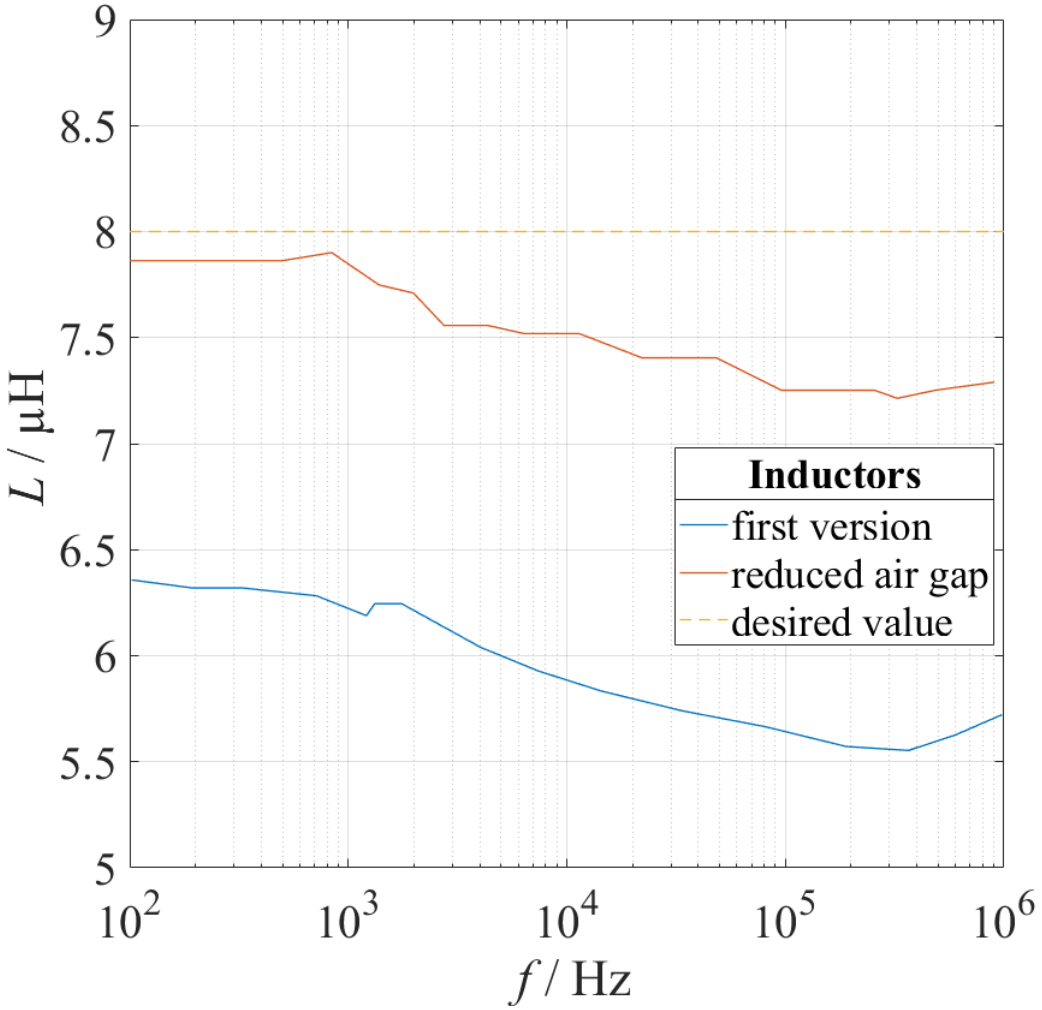

Figure 5.10.: Plot of the measured inductors

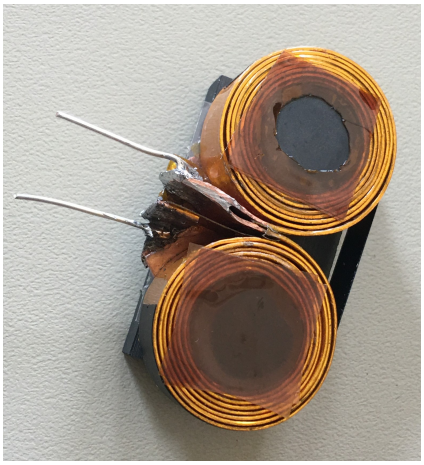

Figure 5.11.: The two ceramic plates are removed and Kapton tape is added. Two extensions are soldered to he inductor to enable a connection to the impedance analyser.

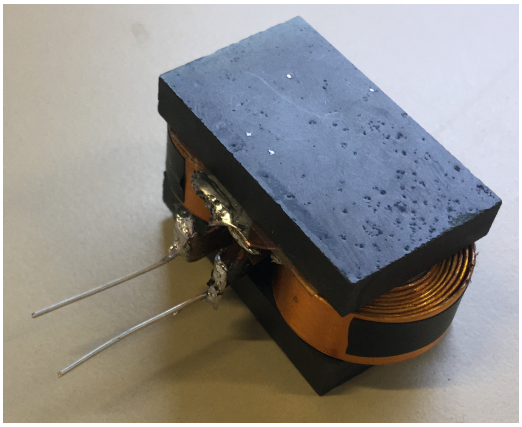

Figure 5.12.: Here a finished inductor is shown.

5.3. Conclusion and Outlook

In this chapter the build up process of the inductors is described and a rebuild of the same or different shaped inductors should be possible by following the basic steps from above. The use of the CNC-Machine allows precise dimensions of the inductances and is much faster. Also, the exposure to harmful dust while cutting the ferrite material by hand could be avoided.

6. Overview of the Cascade Control of the DC/DC Converter

The following is a brief overview of the functionality of the cascade control of the DC/DC converter. This short introduction serves for a better understanding of the programming code. A more detailed description and derivation can be found in the script of the Power Electronics course [20] and the project reports from SS18 [21] and WS19/20 [22].

6.1. Cascade Control

The cascade control of the DC/DC converter consists of an inner current control and an outer voltage control. The block diagram of the cascade control is shown in Figure 6.1.

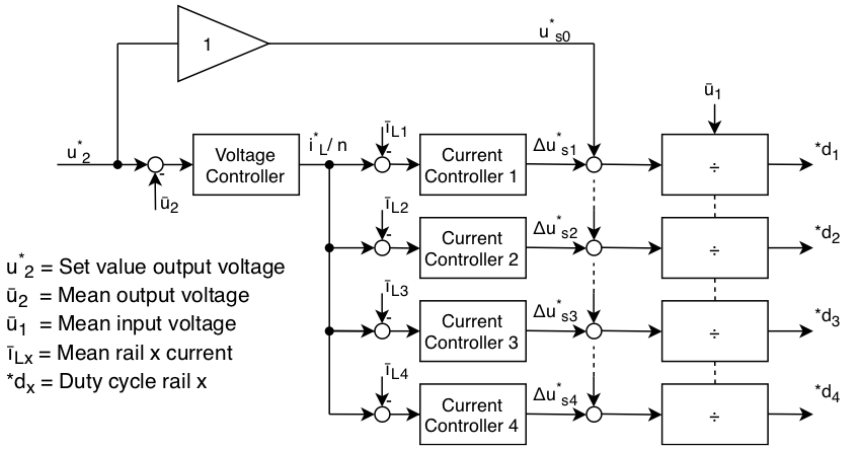

Figure 6.1.: Block diagram of the four times interleaved cascade control for the DC/DC converter

Inner Current Control

The inner current control is designed as a P-controller and controls the current of the half-bridge. A P-controller has a better dynamic behavior compared to the PI-controller and the steady-state control error may deviate from zero. Figure 6.2 shows the block diagram of the inner current control.

$$G_{\mathrm{ci}}(z) = K_{\mathrm{pc}} \tag{6.1}$$

$$G_{\mathrm{i}}(z) = \frac{\frac{K_{\mathrm{pc}} T_{\mathrm{c}}}{L}}{z^2 - z + \frac{K_{\mathrm{pc}} T_{\mathrm{c}}}{L}} \tag{6.2}$$

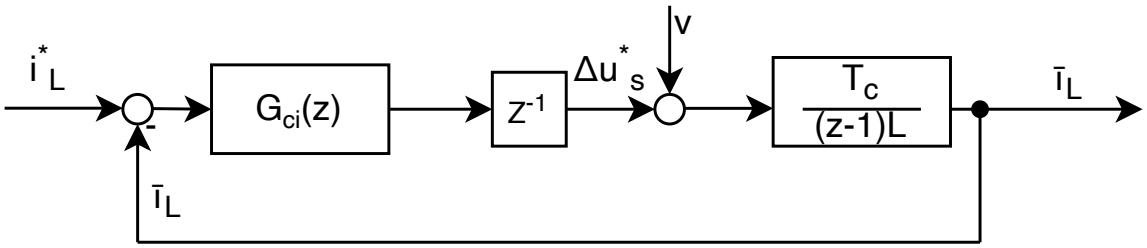

Figure 6.2.: Block diagram of inner current control

Outer Voltage Control

For the outer voltage control, a PI-controller is used to control the output voltage of the converter. This type of controller is used because a steady-state control error of zero is desired. Figure 6.3 shows the block diagram of the outer voltage control.

$$G_{\mathrm{cu}}(z) = K_{\mathrm{pu}} + K_{\mathrm{iu}} \frac{T_{\mathrm{c}}}{1 - z} \tag{6.3}$$

$$G_{\mathrm{u}}(z) = \frac{G_{\mathrm{cu}}(z) G_{\mathrm{i}}(z) \frac{T_{\mathrm{c}}}{(1-z)C_2}}{1 + G_{\mathrm{cu}}(z) G_{\mathrm{i}}(z) \frac{T_{\mathrm{c}}}{(1-z)C_2}} \tag{6.4}$$

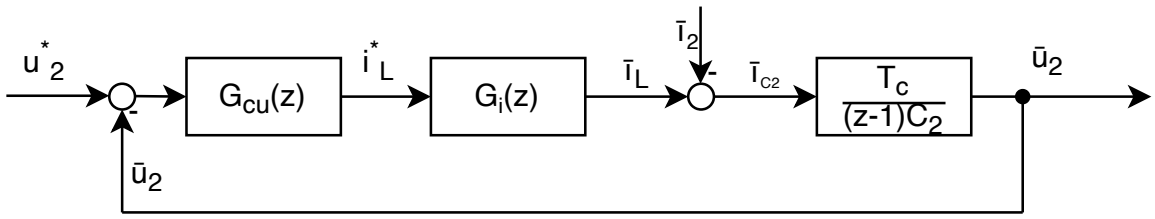

Figure 6.3.: Block diagram from outer voltage control

6.2. Implementation of the Cascade Control on the Microcontroller

Both C2000 microcontrollers have four PWM modules [23] [24] to drive the four rails of the converter. The four PWM units are operated phase-shifted in symmetrical mode. The PWM units can start the voltage measurement of an ADC pin when exceeding or falling below a threshold value. The ADC measurement of the respective rail current starts as soon as the high side MOSFET of the half bridge changes from the conducting to the off state (regular sampling). The ADC unit triggers an interrupt service routine (ISR) of the inner current control when the measurement is finished. In the inner current ISR the new duty cycle for the rail is calculated. The CPU timer starts the interrupt service routine for the outer voltage control. Within the outer voltage ISR the update/calculation of input voltage, output voltage, overvoltage detection, undervoltage detection, target rail current, rail number and switching frequency adjustment is done. The interrupt service routine of the outer voltage control has a lower priority than the inner current control, so it can be interrupted by the inner current control. In the endless loop of the main program an optimization function can be called, which can be interrupted by both interrupt services routines. Within the optimization function it is tried to achieve the efficiency of the converter by adjustments in the switching frequency and rail number.

6.3. Firmware

Remarks Software

The code of the WS19/20 project group was used as the basis for the microcontroller firmware. Due to the Corona pandemic, the previous project group was not able to test the code on the real DC/DC converter ver. 10.0.

For the new 2 kW DC/DC converter, a new control card had to be used because the 100-pin dim connector (Molex 876301001) for the TMDSCNCD28335 Control Card is no longer manufactured. The new Control Card (TMDSDOCK28379D) is based on the TMS320F28379D microcontroller, which is significantly different from TMS320F28335 microcontroller. Since the microcontroller code was implemented close to the hardware for the best performance of the control, the code had to be adapted for the new MCU. To simplify porting of the control code in case of future changes of the microcontroller architecture, a Hardware Abstraction Layer (HAL) was introduced. Figure 6.4 shows the block diagram of the hardware abstraction layer. Here, the control code is almost completely free from hardware-specific functions and uses the HAL functions instead. This has the advantage that when the microcontroller architecture is changed, only the HAL functions need to be rewritten without having to make any changes to the control code. For better readability and maintenance of the code, the code has been repartitioned. Hardware-specific functions are now in only one file. The previous control code contained inner current control, outer voltage control, and optimization functions in only one file. These three functional units have now each been split into separate files.

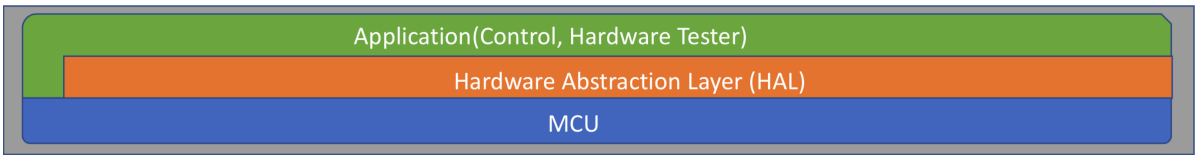

Figure 6.4.: Concept of the Hardware Abstraction Layer (HAL)

Hardware Differences

Unlike the TMS320F28335, the TMS320F28379D has four ADC units instead of just one [23] [24]. This allows all four ADC units to trigger an interrupt independently. Whereas with the TMS320F28335 the rail current measurement is done via only one interrupt service routine. In order to perform several different ADC measurements with one ADC unit, they are executed sequentially. When calling the interrupt service routine (TMS320F28335), the PWM unit for the interrupt must be determined in the first step in order to change the duty cycle of the correct rail. In the previous code of the TMS320F28335 the synchronization of the rail current measurement was ensured by passing on the pointer address. To make the code more portable between the different microcontrollers, the synchronization of the rail current measurement on the TMS320F28335 is ensured by reading out the ADC sequence. No degradation in the execution time was detected by these changes. The synchronization of the rail current measurement happens on the TMS320F28379D by the respective interrupt service routine. It is recommended by the manufacturer to operate these evenly and synchronously with several ADC units [24].

Overcurrent detection on the converter with the TMS320F28335 is performed by an external circuit. This circuit consists of a comparator that compares the voltage output from the current amplifier and the reference voltage. The output of the comparator can disable all half-bridges immediately due to the level changes from high to low. The same overcurrent detection is done by the XBAR internally on the MCU of the TMS320F28379D, so that components could be saved here.

Possible Improvements and Extensions of the Firmware

This project work focuses on a structured and portable control code. The next project group should revise the existing but untested optimization loop. For example, the number of rails should not only be selected based on the best efficiency, but also considering temperature, switching frequency and rail current.

7. Hardware Tester

This chapter describes the function and use of the hardware tester code.

7.1. Hardware Tester Firmware

The hardware tester is a minimal firmware for the microcontroller. With the hardware tester, the correct functioning of the half bridges, the current measurement and voltage measurement can be checked quickly and easily. This software should also enable other team members without programming knowledge to check the correct functioning of the board. Furthermore, there is the advantage that possible hardware errors can be detected more quickly, since software errors can be excluded from the control. The hardware tester allows easy modification of the switching frequency, duty cycle, interlock time, enabling and disabling of half bridges. Correct operation or changes can then be verified using the oscilloscope. In addition, the IDE (Code Composer) or GDB can be used to check the current measured values or voltage measured values for plausibility. Furthermore, new hardware functions and extensions can use this firmware as a basis to quickly implement and test the functionality.

8. Altium-Library

This chapter introduces how new components should be created for the Altium library to ensure consistent quality. The advantage of the Altium library is to prevent recurring errors in the footprint. In addition, in-house created parts provide more control over the board design and a Bill of Material (BOM) can be created quickly. In the future, the Altium library will be synchronized via GitLab or GitHub. In the first step, the last changes should be transferred from the remote repository to the own branch. The library consists of two files (X.PcbLib and X.SCHLIB) and the Datasheet folder. The X.PcbLib file contains the footprints. The X.SCHLIB file contains the schematic symbols of the components. In the folder Datasheet all documents from the manufacturer of the components are stored.

8.1. Creation of New Components

Footprint Creation

When creating a new footprint, the manufacturer's specifications in the datasheet should be followed. If it is necessary to make changes, these should be documented. For many standard components, a footprint can be created quickly using the Component Wizard tool (see Figure 8.1). For easier placement of components, the assembly layer can be used. If possible, all components should have a 3D model. The 3D models can be created with a CAD program, provided by the manufacturer or obtained from a database (e.g. 3D ContentCentral). The mechanical layer 29 is used for the assembly drawing layer. Here the outlines should be drawn in and the Designator (command

".Desginator") should be inserted (see Figure 8.2).

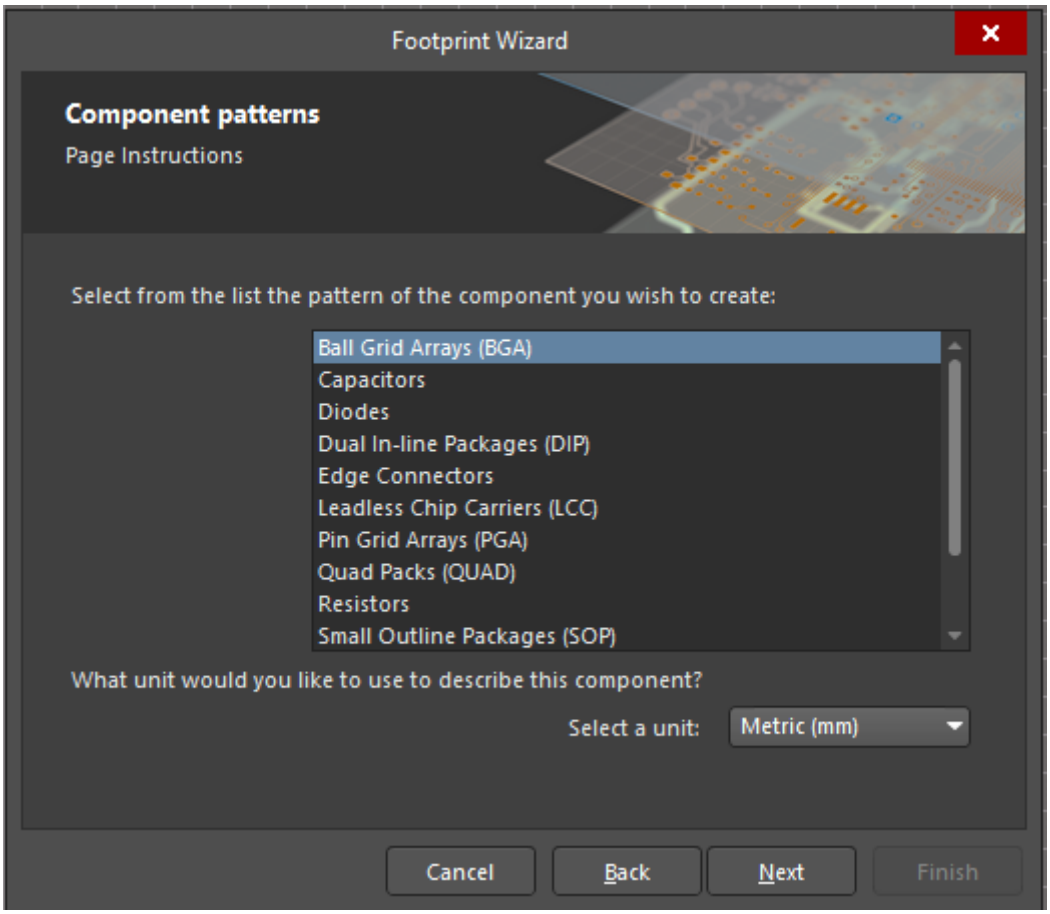

Figure 8.1.: Footprint Wizard window in Altium

Create Schematic Symbols

The schematic symbols should be optimized with regard to the later schematic. For example, supply pins can be placed next to each other. Under the property of the symbol the designator, comments and label can be set (see Figure 8.3). Several footprints can be assigned to one symbol.

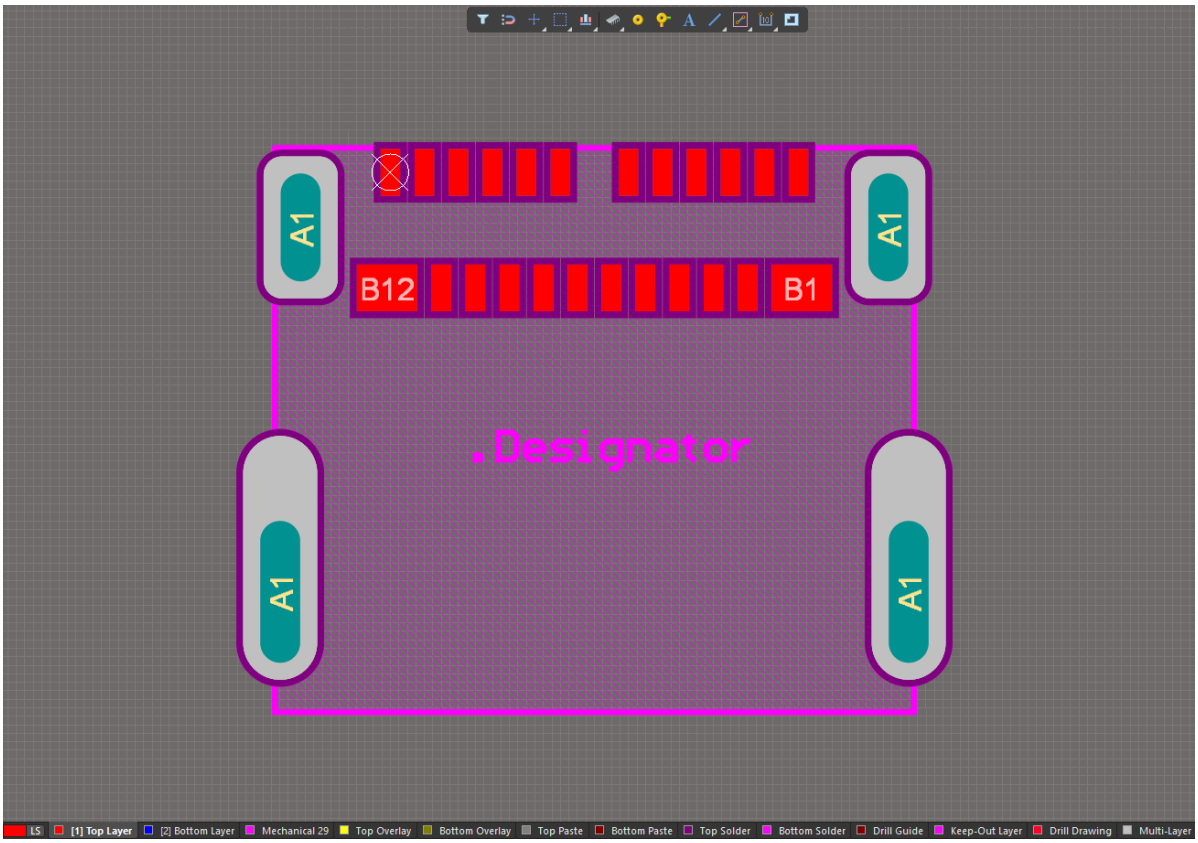

Figure 8.2.: Example of footprint with labeling on layer 29

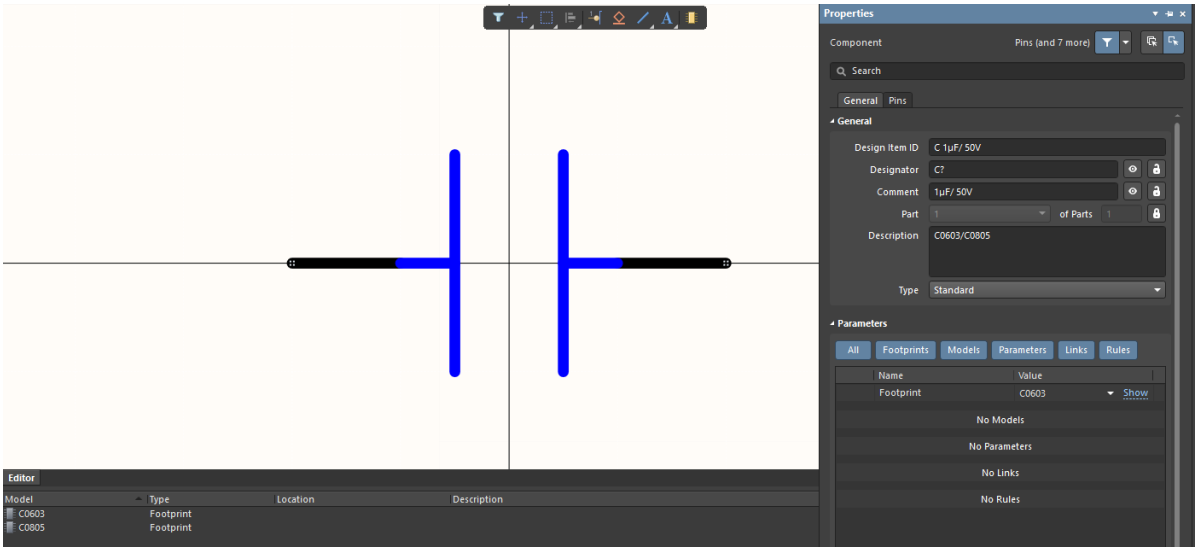

Figure 8.3.: Example of parameter setting of components

9. Measurements of Version 10 Converter

In this chapter the functionality of the DC/DC converter version 10 will be demonstrated. This is done by increasing the output current of the converter to the maximum output power of 1 kW. Furthermore, a long-time test with the maximum output power is done for one hour.

9.1. Experimental Setup

In Figure 9.1 the measurement setup is shown, while Figure 9.2 describes the circuit diagram. The converter is used in buck mode which means the input voltage U_{in} is given as 48 V and the output voltage U_{out} is set by the control to 12 V. For recording the in- and output power along with the efficiency, a power analyzer is used. It measures the voltages u_{in}, u_{out} and the currents i_{in} and i_{out}. While both voltages and the input current could be measured inside the device i_{out} must be determined with a shunt resistor. The reason is the expected maximum current value of 84 A would exceed the devices current sensing input maximum [25]. As a shunt a 1 mΩ resistor was used. The current sensing of i_{in} and i_{out} is in the grounded path because it allows an easier build up even though the input of the measurement device would allow to use the shunt resistor/internal current sensing in the ungrounded path.

Also, the voltages of all rails and the currents of rails 1 and 2 are measured with an oscilloscope to examine differences which could arise during the increase of power.

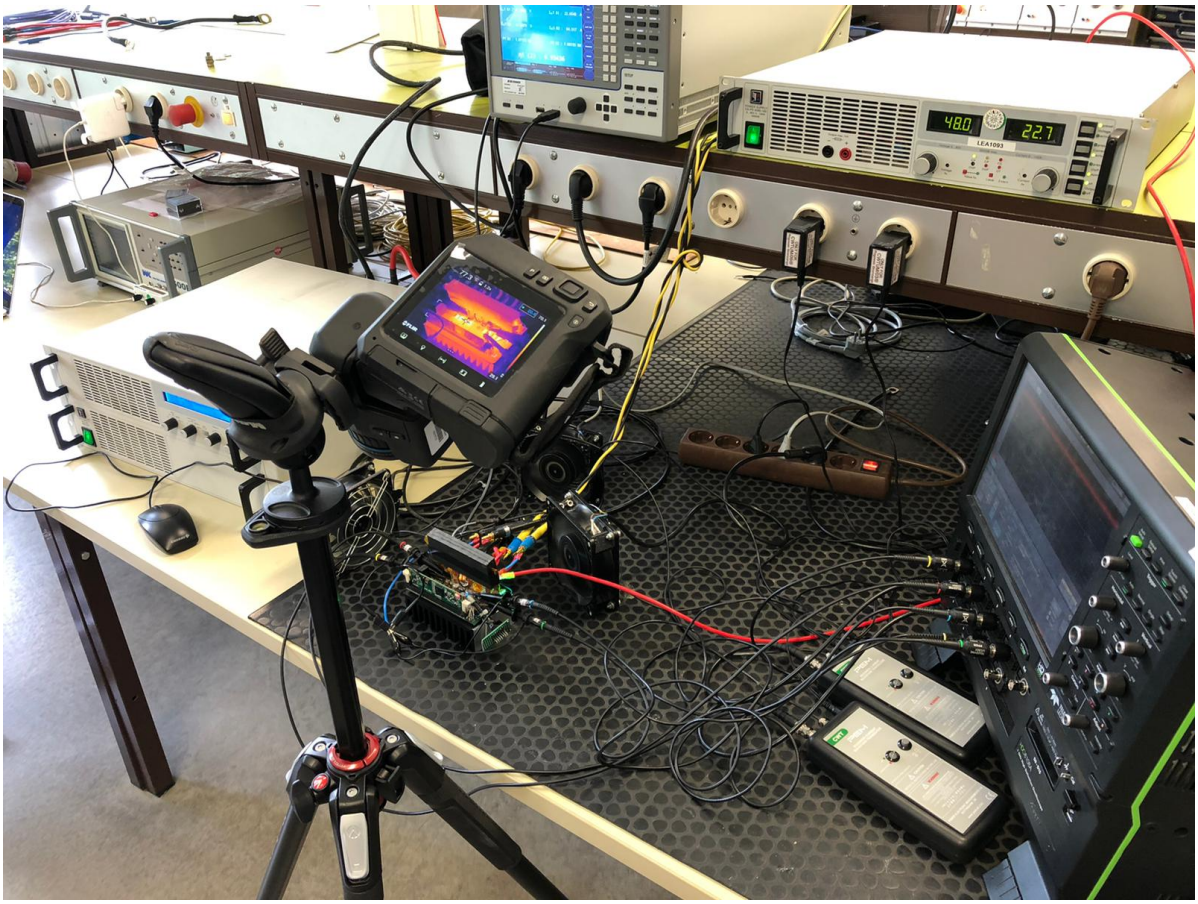

Figure 9.1.: The experimental setup in the lab.

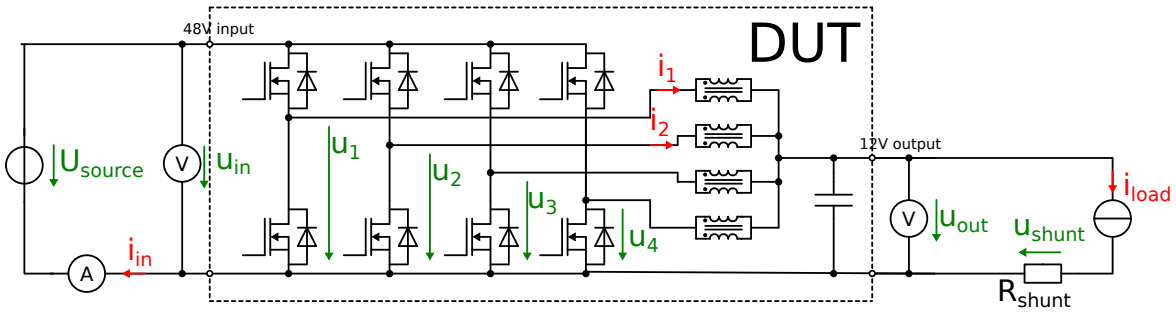

Figure 9.2.: Experimental setup of version 10 DC/DC-converter as Device under Test (DUT).

Unfortunately, just two current values could be measured at one time because only two current sensing devices (Rogowski coil) were available. Finally, the output voltage u_{out} of the converter is recorded with the oscilloscope to evaluate if the used control can ensure an even value of 12 V at different output currents. The Devices used in this setup are:

- Power Supply EA-PS 9080-100 from EA [26]
- Electronic Load EA-EL9400-100 from EA [27]
- Oscilloscope HDO8108A from Teledyn Lecroy [28]
- Power Measurment Device LMG 640 from ZES [25]
- Rogowski coil CWT Ultra-mini from PEM [29]
- Thermal camera from FLIR [30]

To operate the converter, its temperatures must be kept below the maximum limits. This is guaranteed by mounting a heat sink to the board.

9.2. Implementation

As mentioned above, the input voltage U_{in} of the converter is set to a constant value of 48 V by the voltage source. The current i_{out} of the current source is adjusted, so that the output power of the converter, measured via u_{out} and i_{out}, is increased from 0 W to 1 kW. At every step of 50 W the values of the oscilloscope are saved along with a picture of the thermal camera. Because it was assumed, that the efficiency value will vary more at lower power, it was decided to capture this data every 10 W step and after reaching 200 W of output power to do so every 25 W step. After one hour at an output power of 1 kW the temperature of the MOSFETs, ferrite and FR4 material was measured. At this time the temperatures reached a constant value with an ambient temperature of 26.6 °C.

9.3. Evaluation

In Table 9.1 the measured temperatures are listed along with the maximum value they must not exceed.

	Maximum value	Measured value
Ferrite N95	220 °C	43 °C
PGaN MOSFET	150 °C (junction)	77.4 °C (case)
FR4 (PCB material)	110 °C	58 °C

Table 9.1.: Quantities of the different regions for the calculation of the thermal resistances

Because all temperatures lie below their maximum, the heat dissipation of the heat sink seems to be sufficient. Instead of a direct measurement of the MOSFETs junction temperature, the case temperature was measured.

Unfortunately, the thermal simulations of the converter were made with a liquid-cooled housing which is not possible to use due to a missing liquid-cooling system in the lab. The main difference to the heat sink is the constant temperature of the liquid with 60 °C and the fact that the ferrite will be cooled from the top [1]. The enclosure of the board prevents convection, while this is one path for dissipation of thermal energy with the heat sink setup.

Besides the thermal behaviour of the version 10.0 converter, its efficiency

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{u_{\text{out}}^2 / R_{\text{shunt}}}{u_{\text{in}} i_{\text{in}}} \tag{9.1}$$

is measured (see Figure 9.2). This can be compared to the previous DC/DC converters in Figure 9.3. It is obvious that the efficiency of the analysed converter is slightly less than from version 8.0 and 9.0 for a power of 300 W. Referring to the documentation of the WS19/20 group [22] the goal was to build a converter with the same efficiency as the former versions but with an increased power density. Although the efficiency is nearly the same as before, it is pointed out that the power density is increased by 20 %

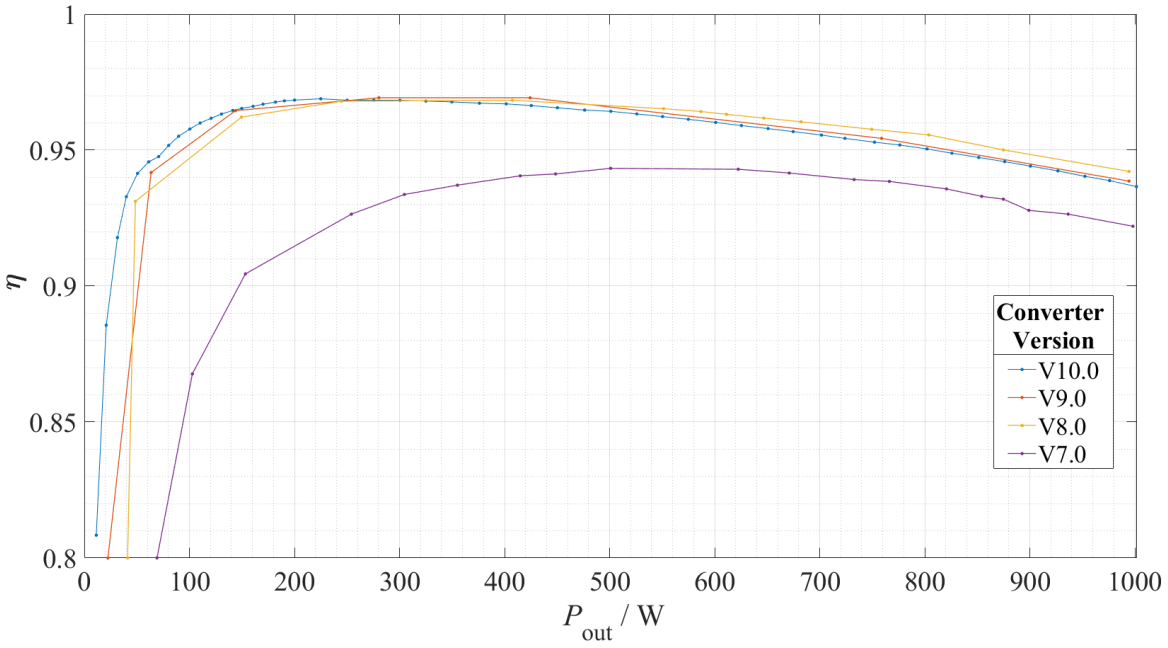

Figure 9.3.: Efficiency of the DC/DC converters

from 1.37 $\frac{\text{kW}}{\text{dm}^3}$ from version 9.0 to 1.64 $\frac{\text{kW}}{\text{dm}^3}$ from version 10.0.

Converter Version	η_{max}	$\eta_{1\text{kW}}$
V10	0.969	0.937
V9.0	0.969	0.939
V8.0	0.942	0.968
V7.0	0.943	0.922

Table 9.2.: Configuration with lowest total loss

10. Description of the WS19/20 DC/DC Board Version 10.0 Errata

In the following section, the known hardware errors of the DC/DC converter of the winter semester 2019/2020 version 10.0 are discussed. Additionally, possible solutions/improvements are presented.

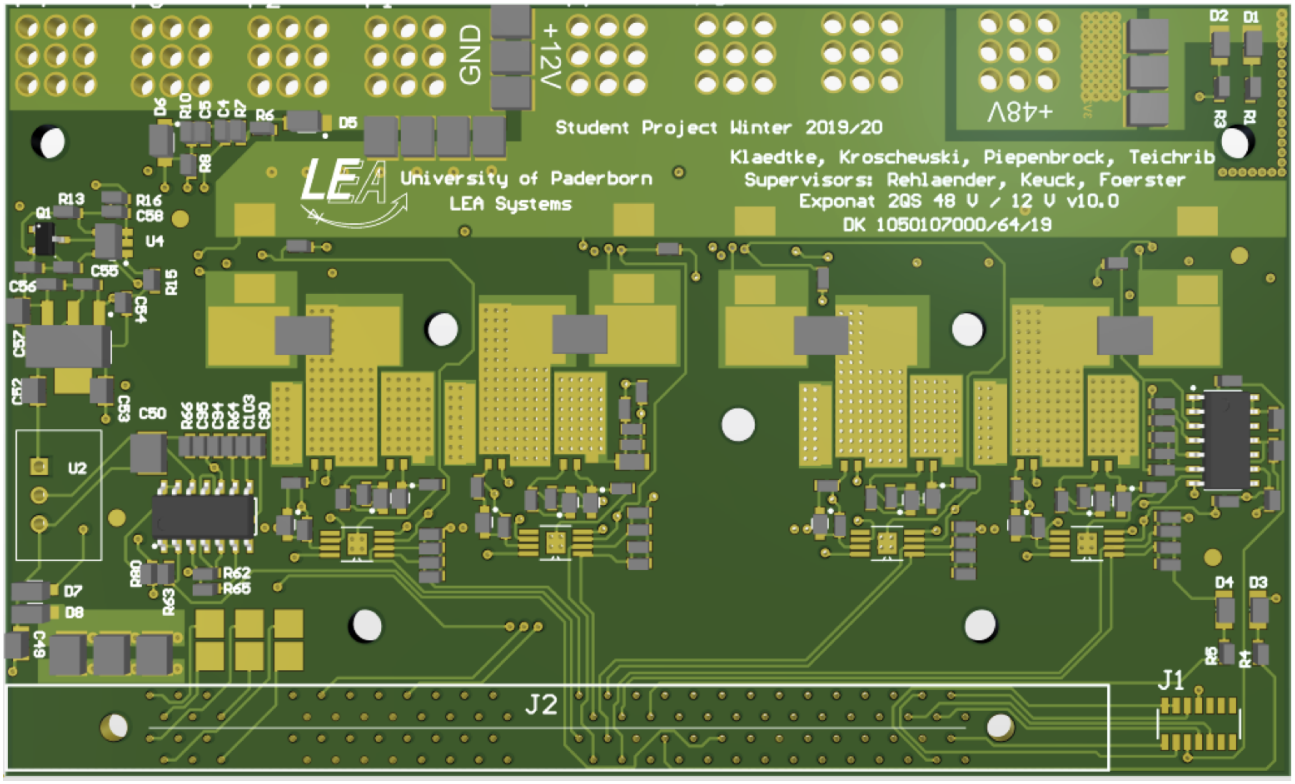

Figure 10.1.: DC/DC Converter Ver. 10.0 PCB

Preliminary Remark

It should be noted that version 10.0 is not the tenth iteration of the same converter, but the tenth DC/DC converter from the department. The DC/DC converter WS19/20 version 10.0 was still built by the previous project group in SS20, but could not be put into operation due to the Corona pandemic. During the attempt to take the converter into operation, errors were discovered by the previous [22] and current project group. For better documentation and to solve the bugs, all version 10.0 bugs are summarized here. With some limitations the DC/DC converter version 10.0, could be operated successfully at a permanent output power of 1 kW for more than one hour.

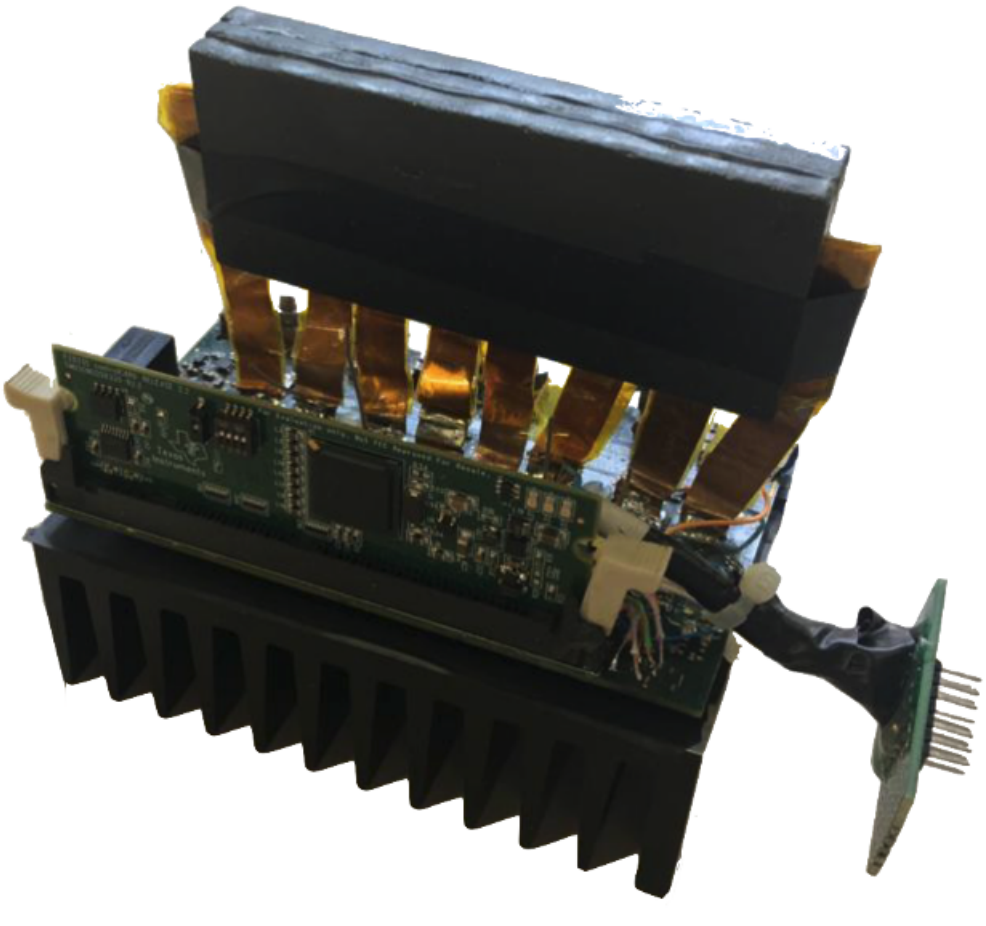

Figure 10.2.: DC/DC Converter Ver. 10.0 with heat sink

10.1. Missing Connections

The measurement of the input voltage and output voltage is performed via two independent voltage dividers (input voltage 48V: R8 and R10. Output voltage 12V: R6 and R7). Unfortunately, the ground of both voltage dividers was not connected to that of the converter (see Figure 10.3). This makes it impossible to measure the voltage across the respective resistors. As a workaround, the missing connection of the grounds was connected with a enamelled wire.

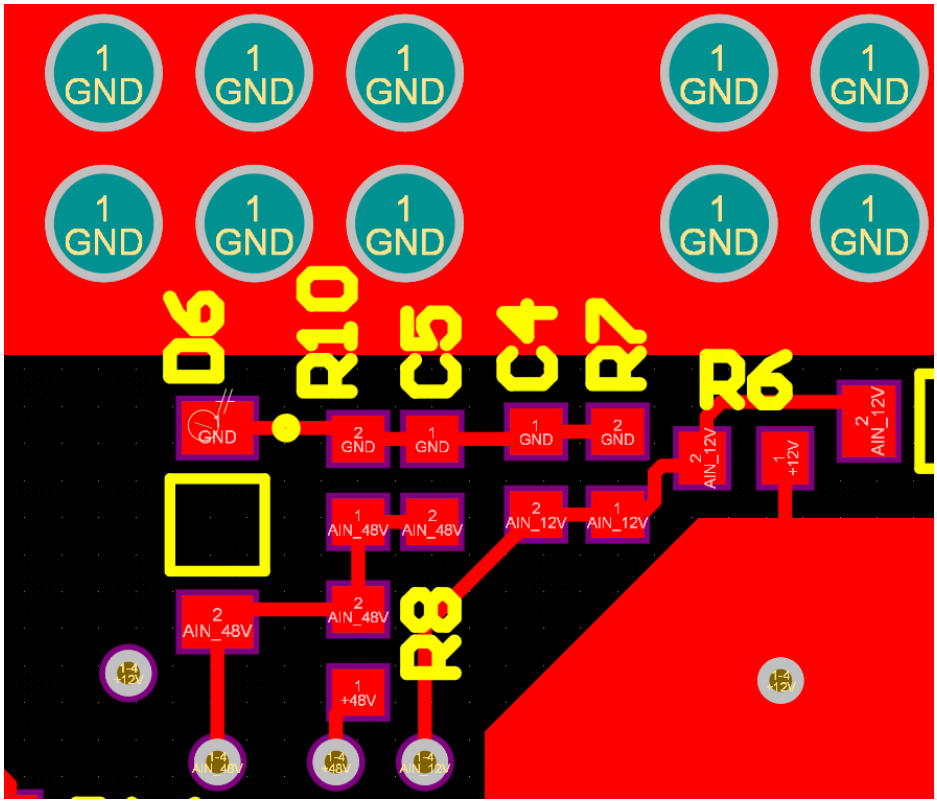

Figure 10.3.: Missing ground connection for the voltage divider

The LED D1 lights up as soon as a voltage is applied to the output of the converter. Unfortunately, a line was also forgotten here during the board layout. To ensure functionality, a connection must be made between the output and resistor R1 (see Figure 10.4).

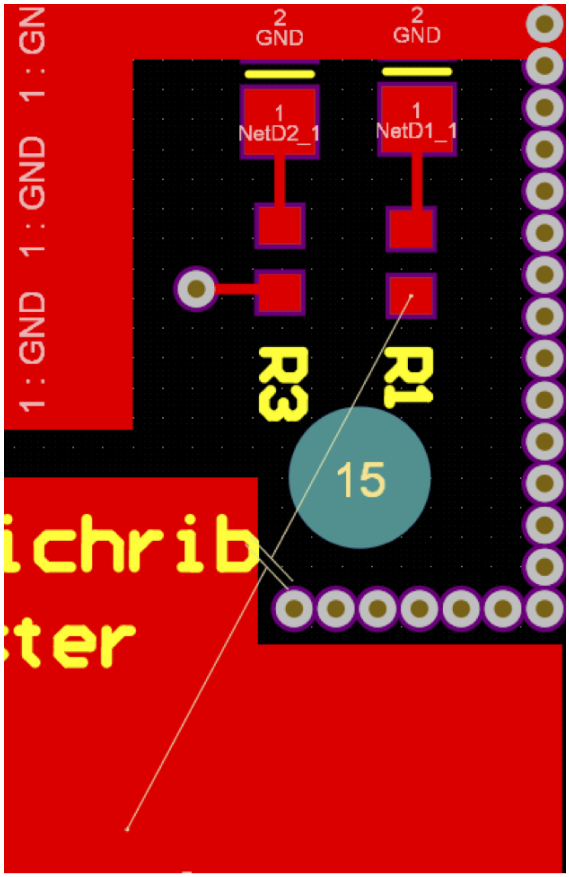

Figure 10.4.: Missing connection to the output voltage from the converter for the status LED

In addition, during the first operation of the converter, it was noticed that the current value of Rail2 permanently displayed a current of −32.98 A (ADC value 4095). This was caused by the fact that the current amplifier could not measure a voltage drop across the shunt resistor R22, since a connection to the output potential from the converter was missing (see Figure 10.5). The problem was solved by soldering a wire.

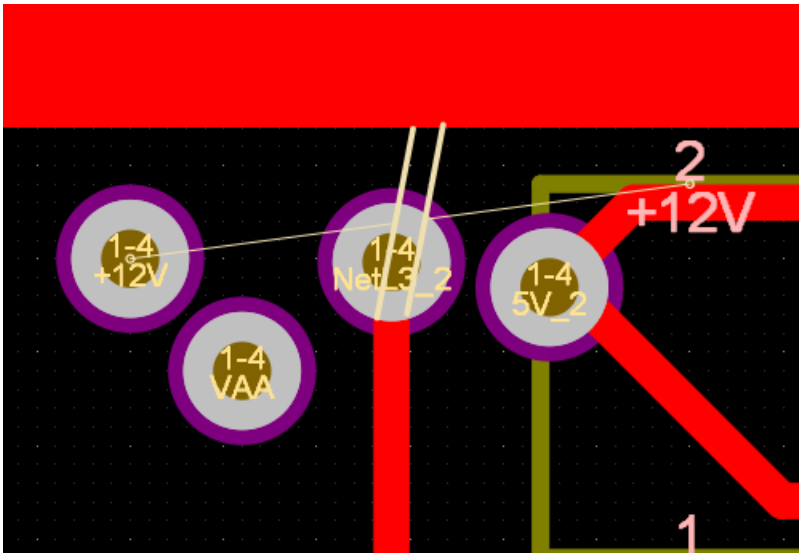

Figure 10.5.: Missing connection to output voltage of converter for current measurement of rail 2

10.2. Error in the Footprint of the MOSFET

When creating the footprint for the MOSFET from GaN Systems model GS61008P, the manufacturer's recommendations were not followed, so that some difficulties resulted during the soldering process. Figure 10.6 shows the manufacturer's recommendations. As can be seen from Figure 10.7, the distance between the drain and thermal pad (connected to source) is only 0.25 mm instead of 0.7 mm. Additionally, no solder mask was provided between the source and thermal pad, and source and coil pad (see Figure 10.8). The MOSFETs are each soldered individually onto the board with the BGA workstation. In the first step, the board and the MOSFET are cleaned and some solder and flux is added to the corresponding pads of the footprint. Then the board is placed in the BGA workstation and the MOSFET is positioned appropriately using a projection. In the last step, the board is heated on the top and bottom side according to the programmed soldering process, while the workstation presses the MOSFET lightly against the board. The heating of the board is accomplished on the top side by a hot air flow. Due to the missing solder mask at the pad transitions, the MOSFET can shift at the end of the soldering process due to the hot air flow. To avoid this displacement of the MOSFET,

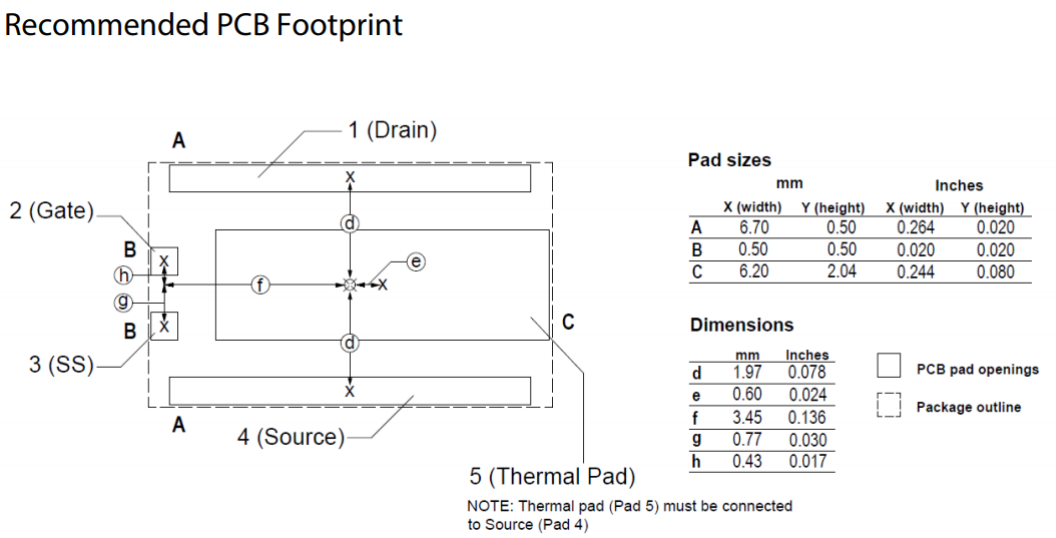

Figure 10.6.: Manufacturer recommendation for MOSFET footprint

solder mask must be applied between the individual pads (see Figure 10.9).

Note Thermal Impact on the MOSFETs

The correct positioning and operation of the MOSFETs could only be validated by switching the respective half bridge. Here the half bridge can be operated for example with the hardware tester presented above. The displacement of the MOSFET during the soldering process unfortunately occurs very often. Figure 10.10 shows the effects of an incorrectly positioned MOSFET. Desoldering and re-soldering the same MOSFET solved the problem (see Figure 10.11). Up to the first operation of the DC/DC converter at an output power of one kilowatt, more than 30 soldering and desoldering processes had to be carried out, which put all MOSFETs under severe thermal stress.

Note Soldering Process

In the middle of this semester, a new reflow oven was acquired at the laboratory of the LEA department, so that the future assembly of the board can be carried out using the reflow process. The advantage of this process is that the assembly can be significantly accelerated and, in addition, the thermal stress for all components is greatly reduced, since in the optimal case only one soldering process is necessary.

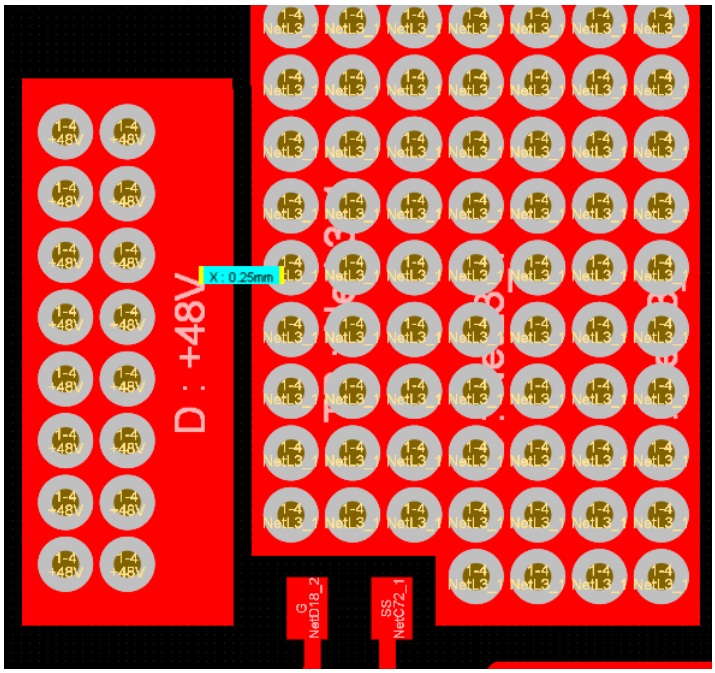

Figure 10.7.: Too small distance between drain pad and thermal pad

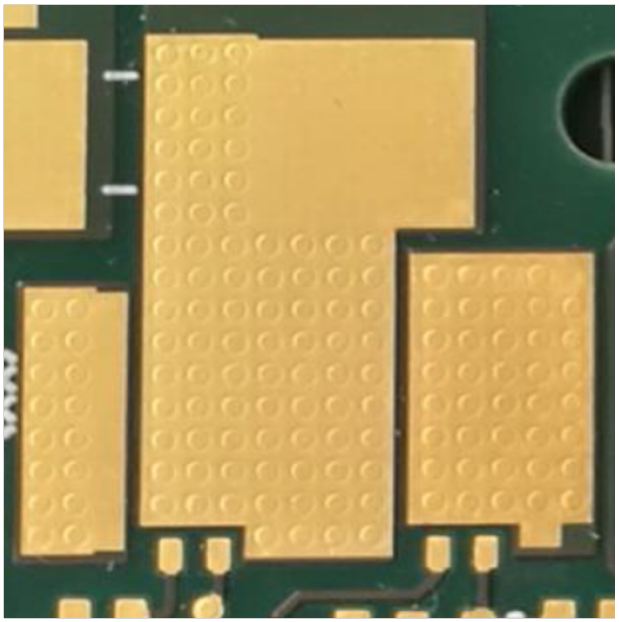

Figure 10.8.: Footprint MOSFET version 10.0 with errors

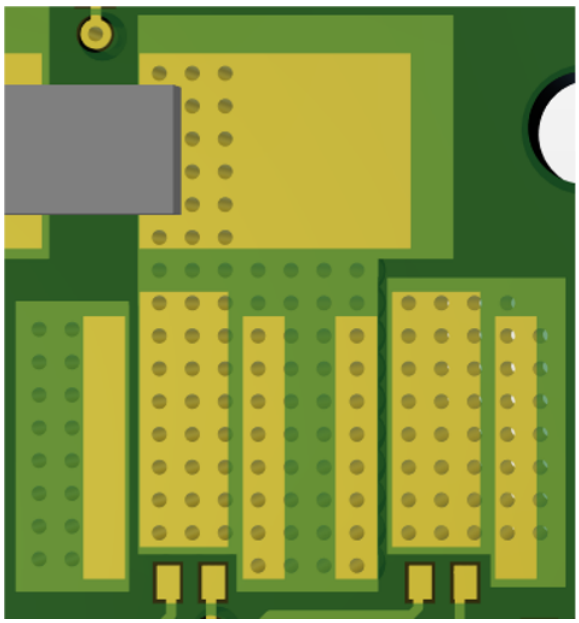

Figure 10.9.: Footprint MOSFET version 10.0 corrected

Figure 10.10.: Half-bridge midpoint voltage with incorrectly positioned high-side MOSFET

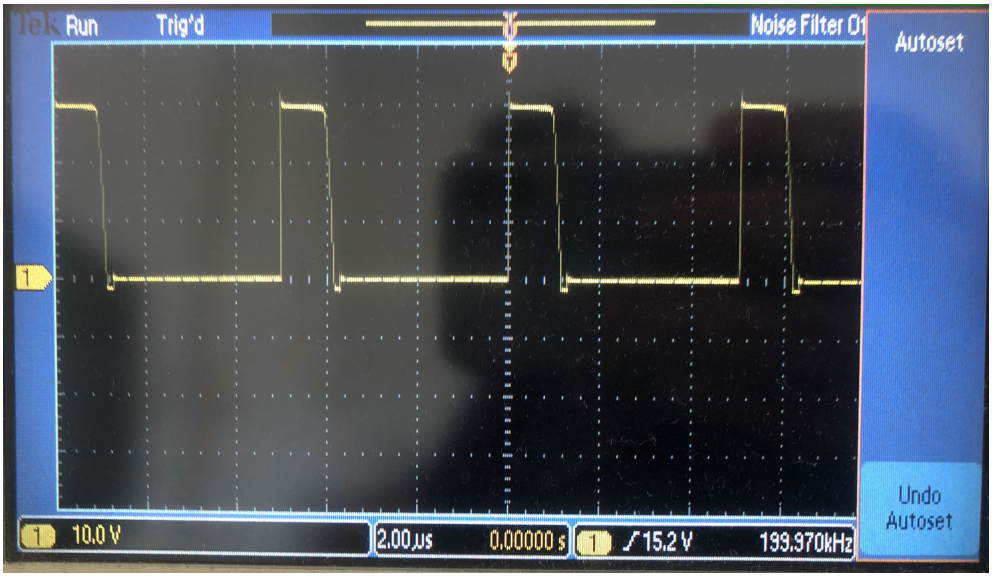

Figure 10.11.: Half-bridge midpoint voltage with same high-side MOSFET but correct positioning

10.3. Error in JTAG Footprint

The JTAG footprint was layouted mirror-inverted in the DC/DC converter V.10 (see Figure 10.12). The previous project group solved the problem by soldering the TCK, TRSTn and Ground lines directly to the JTAG connector with enamelled wire. This construction was very unstable, which unfortunately caused it to break off over time (see Figure 10.13). An attempt was made to repair the design. Unfortunately, the JTAG cable works very unreliably, so debugging and programming the microcontroller is impossible. Therefore the programming of the microcontroller can only be done with the TMDSDOCK28335. It is therefore not possible to debug the converter during operation.

10.4. Problems Current Measurement

When trying to operate the DC/DC converter with an output power of one kilowatt, noise from the coil was noticed from about around 450 watts. These are caused by constant jumping during the duty cycle. A reduction of the interlock time to 4 cycles

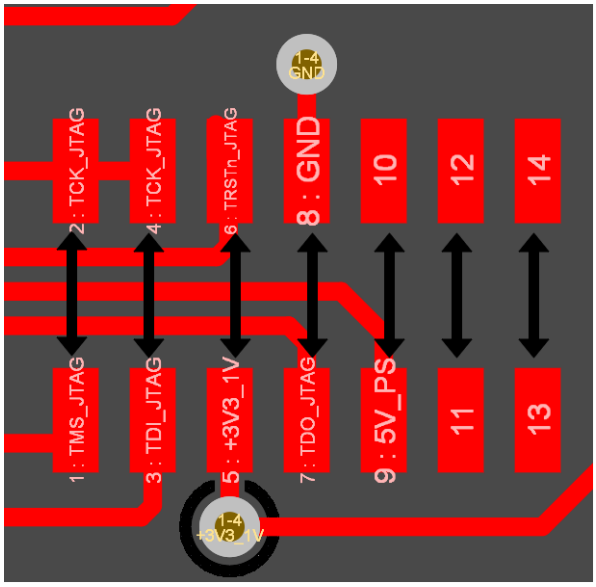

Figure 10.12.: JTAG footprint with swapped sides

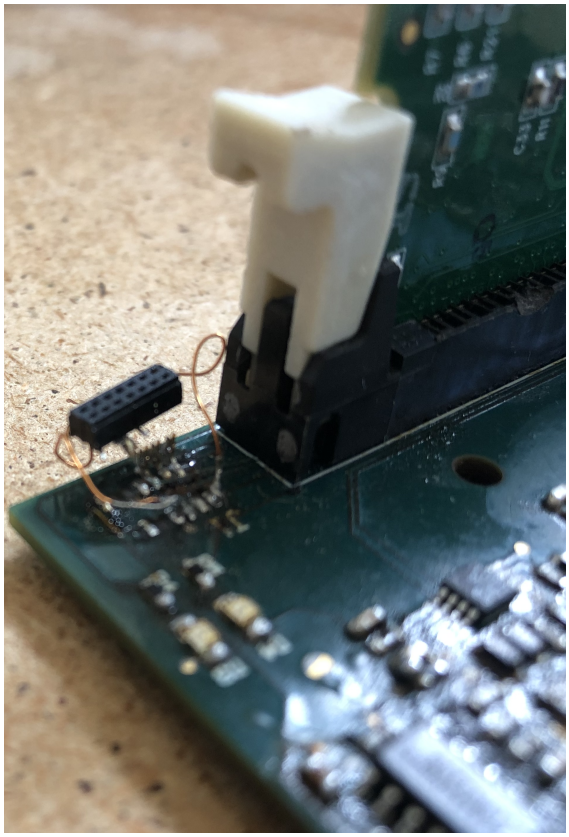

Figure 10.13.: JTAG connection destroyed

(rise and fall time) has made it possible that this effect only occurs from around 800 watts. **Conjecture:** The constant jumping of the duty cycle is attributed to the fact that the maximum current per rail is measured, so that the control limits the current. Current limiting is done by lowering the duty cycle. Once the rail current drops below the maximum value, the duty cycle is increased again. Increasing the maximum current value per rail from 28.0 A to 43.0 A has made it possible to test the converter up to an output power of one kilowatt. Due to the unusable JTAG port, memory could not be accessed from the microcontroller to confirm the assumption. The possibly large measurement deviation can probably be solved by a calibration and an extra filter. In addition, a separate ground (analog ground) should be considered for the measurement of input voltages, output voltages and rail currents.

10.5. Problems with the Coupled Inductors

During the first operation of the converter with all coils, there was damage to the board due to windings that were not well insulated. Inserting the windings into the U-core was only possible with significant pressing, as the insulated windings were too thick. Therefore, all windings were new re-insulated with a thinner Kapton tape. To further reduce the height of the windings, the hole in the winding was enlarged to better fit the ferrite material.

10.6. Problem Short Circuit during Programming

When programming the microcontroller via JTAG, it could be observed from time to time that a short circuit occurs briefly when clearing the memory and thus the input voltage drops. This interrupts the programming process. The error only occurred with the inductor mounted. Due to the non-functional JTAG connection, the cause could not be investigated further.

10.7. Remark at the New Layout of the Board Version 10.0

If the board version 10.0 should be redesigned, then the following points should be considered. The layout of the individual rails should be identical, this simplifies the assembly and debugging of the board significantly. The Altium design rules from this project can be used to simplify and avoid design errors. Furthermore, the cathode side of footprints of diodes should be marked. It is also recommended to rework the footprint of the coils. In addition, attention should be paid to a higher voltage rating of components. (With an input voltage of 48 V, a voltage rating of 50 V is very tight).

11. Description of the WS20/21 DC/DC Board Version 11.0 Errata

In the following section, the known hardware errors of the DC/DC converter of the winter semester 2020/2021 version 11.0 are discussed. Additionally, possible solutions/improvements are presented.

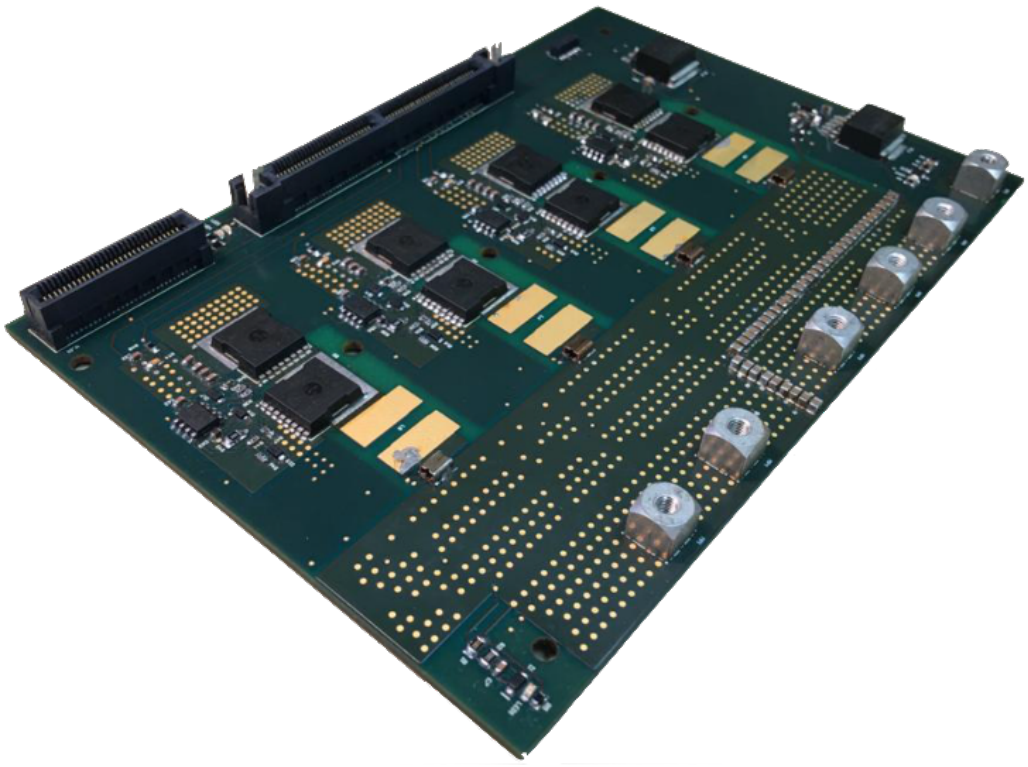

Figure 11.1.: DC/DC Converter Ver. 11.0 PCB

Preliminary Remark

The PCB layout and assembly of the DC/DC converter was carried out by this project group. Shortly after the completion of the assembly, all further tasks necessary for putting into operation were handed over to the next project group. Therefore, other errors in the design cannot be excluded. For the complete overview of all errors of version 11.0, please refer to the future project report SS21. In the following, therefore, only the discovered errors up to the assembly are listed.

11.1. ADC Inputs

As described in the section above, the TMS320F28379D has four independent ADC units each. For best performance, the four ADC units should be loaded as evenly as possible [24]. Unfortunately, this was neglected when creating the schematic. Because of this in version 11.0 of the DC/DC converter WS20/21 one ADC unit measures 9 inputs, others only 2 inputs. A possible solution could look as follows:

- ADC A: I1, I2, I3, I4
- ADC B: $\bar{\text{I}}$1, $\bar{\text{I}}$2, $\bar{\text{I}}$3, $\bar{\text{I}}$4
- ADC C: U1, Temp1, U1, Temp2
- ADC D: U2, Temp3, U2, Temp4

11.2. Error Control Card Connector

When creating the footprint for the control card, unfortunately the numbering of the pins was mixed up (see Figure 11.2). Due to this error it was not possible to mount the Control Card into the HSEC180 connector. This was fixed by modifying the connector. Although the connector is modified, it is not possible to access pins 57 to 64. Since

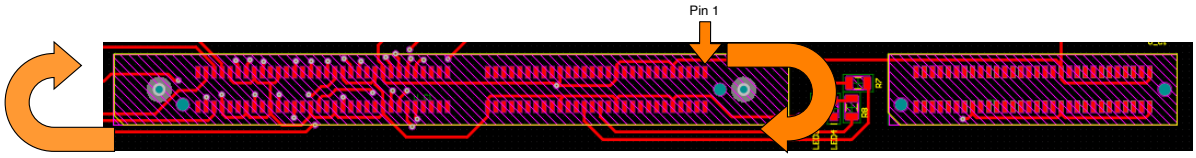

Figure 11.2.: Control Card Footprint error

these pins are not used in version 11.0 of the converter, this error does not result in any restrictions.

11.3. Remark at the New Layout of the Board Version 11.0

The existing JTAG connector on the PCB of version 11.0 is not necessary because the Control Card has an isolated debugger (XDS100). It is therefore possible to remove this JTAG connector with the next revision (11.1). This can save some space on the PCB.

12. Abstract

The design of 2 kW bidirectional DC/DC converter version 11.0 of SS2020 was continued by this semester group. The focus of the project is to finish the converter design, that includes thermal analysis, design and construction of mechanical housing, PCB layout, programming the new control card and further optimization of inductor topology. Along with the design of the converter, the 1 kW version 10.0 converter is built up and tested in the lab. Furthermore, the assembly of the 2 kW converter version 11.0 was finished during this semester but could not be tested due to time constrain and would be carried forward by the new semester group.

The layout was completed considering current ratings and respective temperature rise limitations. The printed circuit board (PCB) is designed such that it would be capable of conducting 42 A current per rail and 167 A of full load output current, with the temperature rise limited up to $\Delta T = 30\,^{\circ}\mathrm{C}$ in an ambient temperature of $T_{\mathrm{a}} = 60\,^{\circ}\mathrm{C}$. The placement of the components especially the MOSFETs along with the gate driver were optimized to save space on the PCB and hence the cost. Also a 6-layer stack-up was chosen to reduce the cost of the PCB. The final PCB dimension is $151\,\mathrm{mm} \times 101\,\mathrm{mm}$.

The thermal analysis of the version 11.0 converter is done with the open source software *Sparselizard* for the first time. The objective is to check if the temperature rise of the MOSFETs is critical and to investigate which model complexity of the PCB is needed to obtain accurate results by simulating different models of the PCB. The simulation results show that the MOSFETs are far below the critical junction temperature. Furthermore, the results lead to the recommendation to replace the thermal vias and the PCB by simple boxes because it saves time, computational effort and provides accurate results.

The design of the housing has to consider some requirements: It must be dust- and waterproofed and shall be compact and lightweight. Also a liquid cooling is developed for the housing. The liquid and electrical connectors shall be commonly used in automotive applications for an easy integration into already existing systems. The housing in this project is designed in such a way that the production is easy and cheap. Due to saving of material during the milling process, it is more sustainable, too. Since this is the first version of the 2 kW converter and improvements are not done yet, the power density is decreased in comparison to previous converters.

The inductor topology was optimized considering the losses and dimensions of core and winding as a cost function. Various configurations, obtained by varying the turns, width of winding and core were simulated using transient analysis and core and copper losses were plotted for comparison. A geometry with lowest losses and lower core volume could be selected as the final inductor configuration. The losses of the newly optimized inductor was reduced by 22 % and the ferrite volume was reduced by 31 %. The construction of the inductor would reduce the volume of ferrite used. Decreased losses in the inductor would contribute to the increased efficiency of the converter.

A new control card is used for the 2 kW converter so the control code is transferred to it. This is easily done by implementing a Hardware Abstraction Layer (HAL) which makes the control code independent from the used microcontroller.

Although the converter version 10.0 was built up by the previous group, it was tested in this project. Besides the measurement of the efficiency, the converter was kept in operation for one hour at full load. The full load efficiency was measured to be 93.7 %. The measurement of the converter shows that its efficiency is comparable to the last converters.

The 1 kW converter of the previous group is built up in the lab. Some problems during this process like missing connections, wrong assembled components, failures in the inductor insulations, errors in the footprint of the JTAG and MOSFETs are corrected.

A. Appendix

A.1. Ansys Electromagnetic Simulation - Configuration List

Label	air gap	leg height	width of winding
a	0.54 mm	22.24 mm	13 mm
b	0.60 mm	20.00 mm	13 mm
c	0.60 mm	23.36 mm	13 mm
d	0.60 mm	22.24 mm	13 mm
e	0.54 mm	20.00 mm	13 mm
f	0.60 mm	21.12 mm	13 mm
g	0.60 mm	21.12 mm	12 mm
h	0.54 mm	26.72 mm	13 mm
i	0.54 mm	23.36 mm	13 mm
j	0.60 mm	24.48 mm	13 mm
k	0.54 mm	21.12 mm	13 mm
l	0.54 mm	24.48 mm	13 mm
m	0.54 mm	27.84 mm	13 mm
n	0.60 mm	25.60 mm	13 mm
o	0.60 mm	20.00 mm	12 mm
p	0.54 mm	25.60 mm	13 mm
q	0.54 mm	28.96 mm	13 mm
r	0.54 mm	20.00 mm	12 mm
s	0.40 mm	21.12 mm	13 mm
t	0.60 mm	27.84 mm	13 mm

Table A.1.: Configurations and their respective labels A

Label	Configurations		
a1	0.60 mm,	22.24 mm,	13 mm
b1	0.60 mm,	22.24 mm,	12 mm
c1	0.60 mm,	22.24 mm,	11 mm
d1	0.60 mm,	24.48 mm,	13 mm
e1	0.60 mm,	24.48 mm,	12 mm
f1	0.60 mm,	24.48 mm,	11 mm
g1	0.60 mm,	26.72 mm,	13 mm
h1	0.60 mm,	26.72 mm,	12 mm
i1	0.60 mm,	26.72 mm,	11 mm
j1	0.60 mm,	27.84 mm,	13 mm
k1	0.60 mm,	27.84 mm,	12 mm
l1	0.54 mm,	27.84 mm,	11 mm
m1	0.54 mm,	22.24 mm,	13 mm
n1	0.54 mm,	22.24 mm,	12 mm
o1	0.54 mm,	22.24 mm,	11 mm
p1	0.54 mm,	24.48 mm,	13 mm
q1	0.54 mm,	24.48 mm,	12 mm
r1	0.54 mm,	24.48 mm,	11 mm
s1	0.54 mm,	26.72 mm,	13 mm
t1	0.54 mm,	26.72 mm,	12 mm

Table A.2.: Configurations and their respective labels B

A.2. Matlab Code for the Geometry Generation

```
% Code generation for the generation of the thermal vias in gmsh
% All values in mm
number = 31;
x0 = 0; y0 = 0; z0 = 2.5;
dx = 0; dy = 0;
nx = 0; ny = 0;
r = 0.325;
h = 1.5;
for j=1:1:7
    if(j==1)
        x0 = 4; y0 = 11.3;
        dx = 1.016; dy = 1.143;
        nx = 4; ny = 9;
    end

    if(j==2)
        x0 = 11.2; y0 = 11.726;
        dx = 1.016; dy = 1.143;
        nx = 4; ny = 8;
    end

    if(j==3)
        x0 = 16.26; y0 = 11.5;
        dx = 0.889; dy = 0.762;
        nx = 12; ny = 11;
    end

    if(j==4)
        x0 = 27.05; y0 = 11.701;
        dx = 1.016; dy = 1.143;
        nx = 2; ny = 8;
    end

    if(j==5)
        x0 = 30.5; y0 = 11.701;
        dx = 1; dy = 1.143;
        nx = 1; ny = 7;
```

```
    end

    if(j==6)
        x0 = 35.3; y0 = 13.468;
        dx = 0.762; dy = 0.889;
        nx = 11; ny = 13;
    end

    if(j==7)
     x0 = 44.319; y0 = 13.97;
     dx = 1.397; dy = 1.397;
     nx = 4; ny = 10;
    end

    for k=0:1:nx-1
        for l=0:1:ny-1
            if ~(j==3 && k==11 && l==10)
                fprintf('Cylinder(%.0f) = {%.3f/1000, %.3f/1000, %.3f
    /1000, 0, 0, %.3f/1000, %.3f/1000, 2*Pi};      \n//+\n',number,x0+k*dx,
    y0-l*dy,z0,h,r);
                number = number + 1;
            end
        end
    end
end

% Code generation for the definition of the physical groups
var_start = 31;
var_end = 435;
for m=var_start:1:var_end
    fprintf('%.0f, ',m);
end
```

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