

Elektronische Stromversorgungen

Übung: Analysis and Design of Phase Shifted Zero-Voltage-Switching Full-Bridge DC/DC Converter

At high power levels the Phase Shifted Zero-Voltage-Switching (ZVS) Full-Bridge DC/DC converter presents an attractive choice. In addition to the constant frequency operation, the switching stress and losses are reduced by soft switching technique.

In this exercise analysis and design considerations are studied for this topology. An overview of this switching technique including the equivalent circuit for each interval, steady-state voltage and current waveforms and supporting design equations are highlighted. A general purpose Phase Shifted converter design guide and procedure is introduced to assist in weighing the various design tradeoffs.

An experimental 500W, 48V at 10.5A power supply design operating from a 400V DC input voltage and switched at f_s 200 kHz is presented as an example. Considerations are given to following aspects: circuit analysis, resonant components design for ZVS, switching loss estimation and control concepts based on current mode control. A summary of comparative advantages, differences and tradeoffs to conventional hard switching full-bridge dc-dc converter is included.

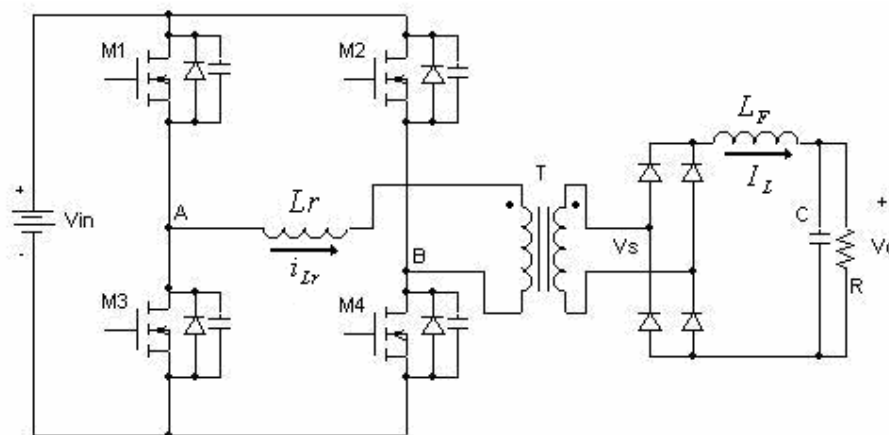


Fig. 1 Phase shifted ZVS full-bridge dc-dc converter

1. Operational analysis and waveforms

An analysis is to be performed yielding equivalent circuits, initial conditions for each time interval and governing equations for the circuit variables listed below:

- 1) Currents and voltages of the transformer primary and secondary side.
- 2) Currents and voltages of switches.
- 3) Currents and voltages of rectifying diodes.

The results of the previous analysis are to be displayed by showing the main operational waveforms.

In order to simplify the operational analysis and emphasize the main principle of the circuit, the following assumptions are made:

- 1) All power semiconductor components are lossless, (i.e. on state resistances are ignored).
- 2) The internal output capacitances of transistors when in off-state are considered in order to calculate the ZVS range of converter.
- 3) The turn-on and turn-off switching of diodes and transistors are considered as ideal (i.e. without delay between gate drive signals and i_{DS} and v_{DS} response).
- 4) The transformer is replaced by an equivalent circuit consisting of a leakage inductance L_s and an ideal transformer T with voltage ratio equal to turns ratio. The magnetizing inductance is ignored as well as core and copper losses.
- 5) The output filter comprising inductor L_F and filter capacitor C_F is ideal. Hence, the output filter L_F , C_F and the load are replaced by a const current source I_2 .

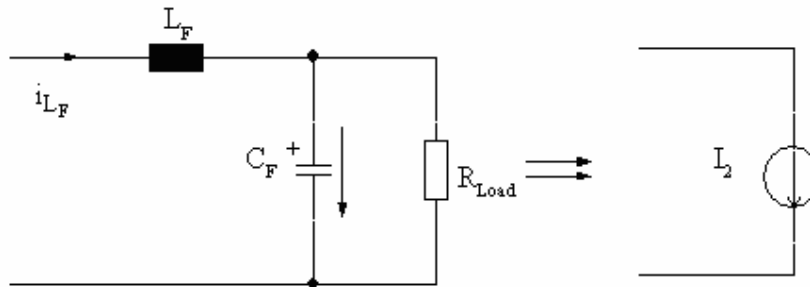


Fig. 2 Output filter circuit

2. Switching conditions

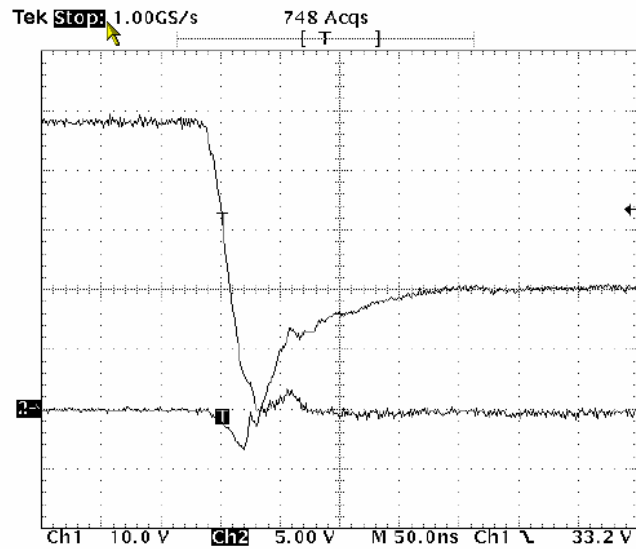
The main highlight of using phase shifted control instead of traditional PWM control is the resulting ZVS of the transistors, allowing switching at elevated frequencies at tolerable switching losses. The ZVS condition depends on the load and some circuit parameters such as transistor capacitances and resonance inductance L_r , consisting of the leakage inductance of the transformer added by an extra inductor ($L_r = L_{ext} + L_s$).

Therefore the switching conditions are to be analysed so that with given transistor capacitances C_{oss} ZVS should occur for a load range of 70% to 100% of rated current. The value for C_{oss} equals 350 pF when using transistor type IRFP450.

Determine the necessary value of L_r , if the input voltage range is 300 - 400V.

3. Switching losses analysis

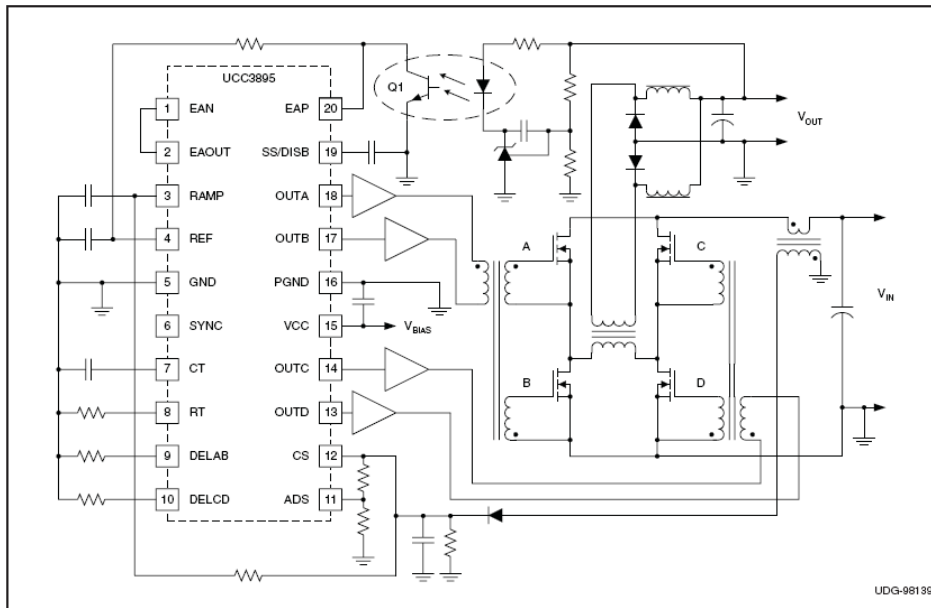
Calculate the efficiency improvement at rated power resulting from the ZVS mode of the primary side transistors as compared to the hard switching converter. An approximative calculation based on simple geometric waveforms and physical reasoning is sufficient neglecting ringing (high frequency oscillations) effects.



4. Introduction to current mode control

Discuss the peak and average current mode control concept using given block diagram for phase controller UC3895 by construction of signal diagrams.

SIMPLIFIED APPLICATION DIAGRAM



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