UNIVERSITÄT PADERBORN
Die Universität der Informationsgesellschaft

NVIDIA CUDA

Bachelor Thesis

Optimize GPU-Accelerated Fault Simulation with Fault Grouping

In today's technology nodes a growing number of chips contain safety-critical components which are used in advanced driver assistance and in future for level 5 full self driving vehicles. The chips used in this area have demanding requirements for long-term reliability which increases the simulation runtime for test validation. Therefore electronic design automation tools are mostly compute intensive when running circuit simulations and result therefore in a bottleneck, when simulated with multi-million gate designs.

Problem statement:

This bachelor thesis focus on implementing an optimized greedy algorithm in C++ that groups parallel computable faults together and therefore optimizes both the runtime of the greedy algorithm and the runtime of the GPU-accelerated fault simulation. Figure 1 shows a simple example of this idea. The evaluation of this work is done by comparing the new implemented algorithm with an existing approach implemented in Java [2].

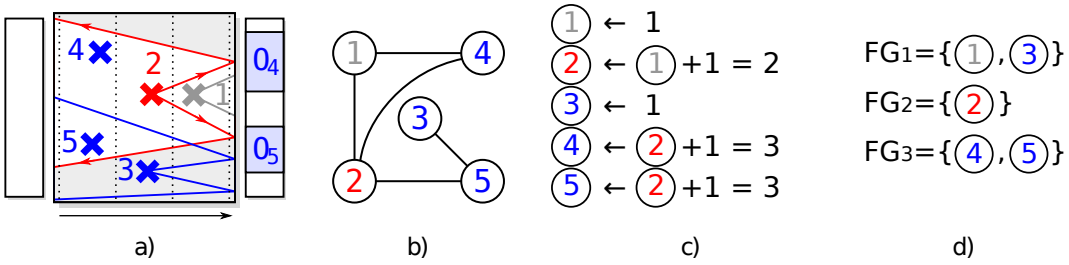

Figure 1: Fault grouping example: a) Fault set F := f 1 , f 2 , f 3 , f 4 , f 5 in reverse topological order, b) output-dependencies, c) group indices and d) resulting fault groups. Obtained from [1].

Solution aspects:

- Literature survey on the problem
- Implement and evaluate both approaches
- Using GPU-Simulation.
- Evaluation of the approach by means of simulation

Requirements:

- Interest in working in a current research project FAST supported by the DFG
- Skills in C++, git, cmake, (a little bit Java)

Literature:

- E. Schneider, "Multi-level simulation of nano-electronic digital circuits on GPUs" - Dissertation, University of Stuttgart 2019
- E. Schneider, S. Holst, M. A. Kochte, X. Wen and H. Wunderlich, "GPU-accelerated small delay fault simulation," 2015 Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, 2015, pp. 1174-1179.

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