Abstract Herr M.Sc. Matthias Kampmann
Built-In Test for Small Delay Faults

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The continuous downscaling of feature sizes in modern process technologies allows to integrate increasingly complex functionality onto a decreasing chip area. While this enables to build highly advanced applications, the risk of producing marginal hardware is increasing as well. Marginal hardware does not result in faulty behavior at the beginning of the product life cycle, but can degenerate into an actual defect quickly. This leads to an early life failure, which can result in catastrophic failures. It has been shown that marginal hardware increases the switching delay by a small amount. Therefore, it can be modeled as a small delay fault. These faults can be detected with a Faster-than-At-Speed Test (FAST), which overclocks the circuit under test in order to make small deviations from specified timing behavior visible. In this talk, the concept of FAST is extended to a built-in self-test (Built-In FAST). It presents an architectural overview and some of the design and implementation challenges that need to be solved for a successful integration. Specifically, this talk highlights the optimal frequency selection problem. Its goal is to determine as few frequencies as possible to detect all possible small delay faults. Furthermore, a design-for built-in FAST technique is presented, that supports test response compaction in the presence of unknown logic values (X-values). X-values are a serious challenge in FAST since outputs can be captured before their computation has finished. In this approach, specialized scan-chains are combined with a simple masking system in order to mask as many Xvalues as possible, before they are fed into the test response compaction. For both parts, results of an extensive simulation study are given that show the feasibility of the presented methods.