Reduction of Total Harmonic Distortion (THD) for Interleaved Converters Operating in Discontinuous Conduction Mode (DCM)

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Abstract

By means of interleaving the total harmonic distortions (THD) can be reduced significantly. At particular duty ratios the harmonics are even totally eliminated. Thus, with specific phase shedding depending on the duty ratio the THD can be further reduced. If converters are operated in discontinuous conduction mode (DCM) the DCM ratio can be used for a continuous phase shedding method where also fractional numbers of energized phases can be applied. This method is used to minimize the THD for the entire duty ratio range also for applications with unequal inductance values.

1. Introduction

Interleaving, characterized by two or more parallel-connected converters operated with phase shifted gate signals, is the preferred technique to reduce the THD and to increase the power level. Typical applications are point-of-load (POL) DC-DC converters and boost power factor correction (PFC) rectifiers [1] [2].

In order to achieve high efficiencies it is popular to operate PFC rectifiers at the boundary between continuous (CCM) and discontinuous conduction mode (DCM). In this boundary conduction mode (BCM) interleaving is challenging due to the varying switching frequency. In [3] a feedforward control method is used which provides optimal interleaving for multi-phase PFC converter operated in BCM. With little effort, DCM with an adjustable DCM ratio can be applied. This DCM ratio can be used for a continuous phase shedding method.

In this paper a strategy is proposed which minimizes the THD in the input current of multi-phase interleaved boost converters by using continuous phase shedding. It is well known that at particular duty ratios the harmonics are totally eliminated. Thus, the THD can be optimized by phase shedding. With continuous phase shedding the number of energized phases is no longer limited to integer values, also fractional values can be applied.

In the following it is described how the adjustable DCM ratio is used for continuous phase shedding. Subsequently it is shown how the THD can be minimized by using continuous phase shedding.

First the situation with equal inductance values is examined, where the optimal DCM ratio depending on the duty ratio needs to be determined. Thereafter the THD optimization for unequal inductance values is presented. Thereto also the phase shifts are adjusted and every phase gets its individual DCM ratio.

2. Continuous Phase Shedding

The feedforward algorithm for BCM and DCM presented in [3] for a PFC boost converter consists of two basic equations which determine the switch on-time T_{on} (1) and the switching period T_s (2).

$$T_{on} = \frac{2L}{v_{in}} \frac{i_{ref}}{n} K_{lag}, \tag{1}$$

$$T_s = T_{on} \frac{v_{out}}{v_{out} - v_{in}} K_{lag}, \tag{2}$$

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where n represents the number of physically paralleled converter and K_{lag} is the DCM ratio. In BCM K_{lag} is equal to 1, while DCM is characterized by $K_{lag} > 1$.

The principle of the conventional phase shedding is that an integer number of phases are completely turned off, while the remaining phases transfer the power. The idea of continuous phase shedding is to keep all phases running, while every phase is only active during a certain ratio of time within the switching period determined by the DCM ratio K_{lag}. The conventional phase shedding with an integer number k of energized phases would correspond to $K_{lag} = n/k$. Unlike the conventional approach k can now be chosen as any real number $0 < k \leq n$ to allow continuous phase shedding. The comparability of continuous phase shedding is exemplified in Fig. 2. It results in equal switching instants and input current shapes like conventional discrete phase shedding.

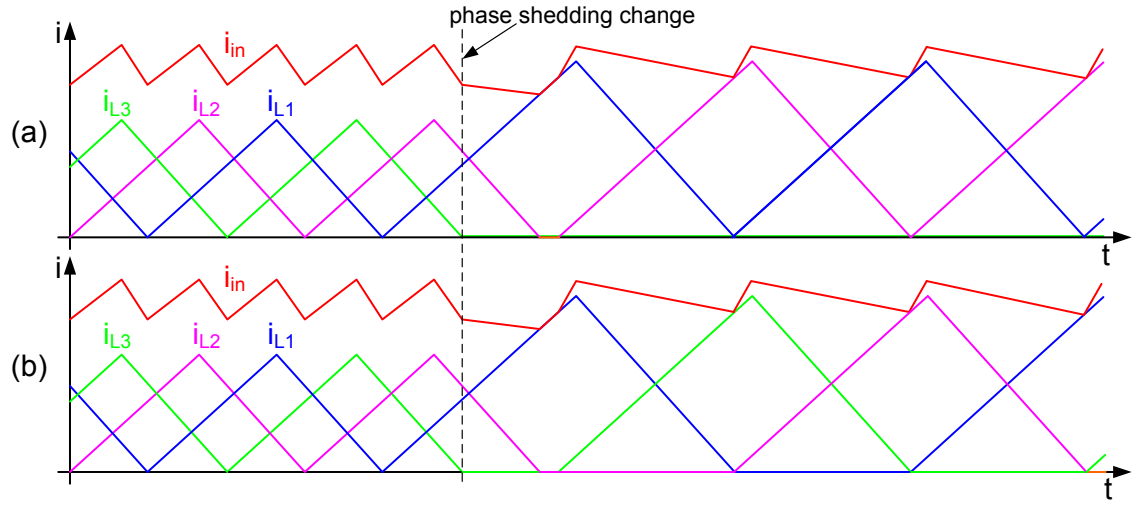

Fig. 1. Total input current and phase currents during phase shedding switching from 3 to 2 phase operation at $\boldsymbol{D = 0.55}$, (a) conventional discrete phase shedding, (b) continuous phase shedding

3. THD Minimization for Equal Inductance Values

3.1. Control Law

One major reason for interleaving several converters is the significant reduction of the input current ripple and the THD. The gain of improvement depends on the number of interleaved phases and the duty ratio [2]. At particular duty ratios D the harmonics are totally eliminated, e.g. with two interleaved phases at $D = 0.5$ or at $D = 1/3$ or $D = 2/3$ with three interleaved phases. Hence, there is the potential to further reduce or to eliminate the THD by changing the number of interleaved phases depending on the duty ratio.

Since the THD corresponds approximately with the normalized input current ripple in this application, this quantity is used as objective in the following. In order to get comparable results for different numbers of interleaved converters a normalized input current ripple is utilized. Therefore the ripple of the input current Δi_{in} is divided by the average of the input current $\bar{i}_{in}$. For $k = 3$ interleaved boost converters operating in BCM the normalized input current ripple as a function of the duty ratio can be expressed as

$$\frac{\Delta i_{in}}{\bar{i}_{in}}(D) = \frac{2}{3} \cdot \begin{cases} \dfrac{1-3D}{1-D} & \text{for } 0 < D \leq \dfrac{1}{3} \\ \dfrac{2-9(D-D^2)}{3(D-D^2)} & \text{for } \dfrac{1}{3} < D \leq \dfrac{2}{3} \\ \dfrac{-2+3D}{D} & \text{for } \dfrac{2}{3} < D \leq 1 \end{cases} \tag{3}$$

For $k = 4$ it follows

$$\frac{\Delta i_{in}}{\bar{i}_{in}}(D) = \frac{1}{2} \cdot \begin{cases} \dfrac{1-4D}{1-D} & \text{for } 0 < D \le \dfrac{1}{4} \\ \dfrac{1-6D+8D^2}{2(-D+D^2)} & \text{for } \dfrac{1}{4} < D \le \dfrac{1}{2} \\ \dfrac{3-10D+8D^2}{2(-D+D^2)} & \text{for } \dfrac{1}{2} < D \le \dfrac{3}{4} \\ \dfrac{-3+4D}{D} & \text{for } \dfrac{3}{4} < D \le 1 \end{cases}. \tag{4}$$

Fig. 2 shows the normalized current ripple versus the duty ratio for $k = 3$ (green) and $k = 4$ (blue) energized phases. It can be seen that the optimal value of k for minimum current ripple changes in the region of $D = 1/3$ and $D = 2/3$ from $k = 4$ to $k = 3$. This fact can be used to create a phase shedding control law for minimum current ripple (cf. Fig. 3 blue curve).

The input current is the sum of the four phase currents. At continuous phase shedding with determined DCM ratio the ripple or rather the THD of the input current has to be analyzed. Hence, a proper method is required to describe the input current in a mathematical way. Well suited for this purpose is the Fourier synthesis. Necessary is the calculation of the Fourier coefficients Q_ν for the phase currents depending on the variables duty ratio D and DCM ratio K_{lag}. The resulting formula to compute the Fourier coefficients is

$$Q_\nu = \frac{\bar{i}_L \, K_{lag}^2}{2\pi^2 \nu^2 D(1-D)} \left[e^{-j\nu D \frac{2\pi}{K_{lag}}} - 1 + D - D\, e^{-j\nu \frac{2\pi}{K_{lag}}} \right]. \tag{5}$$

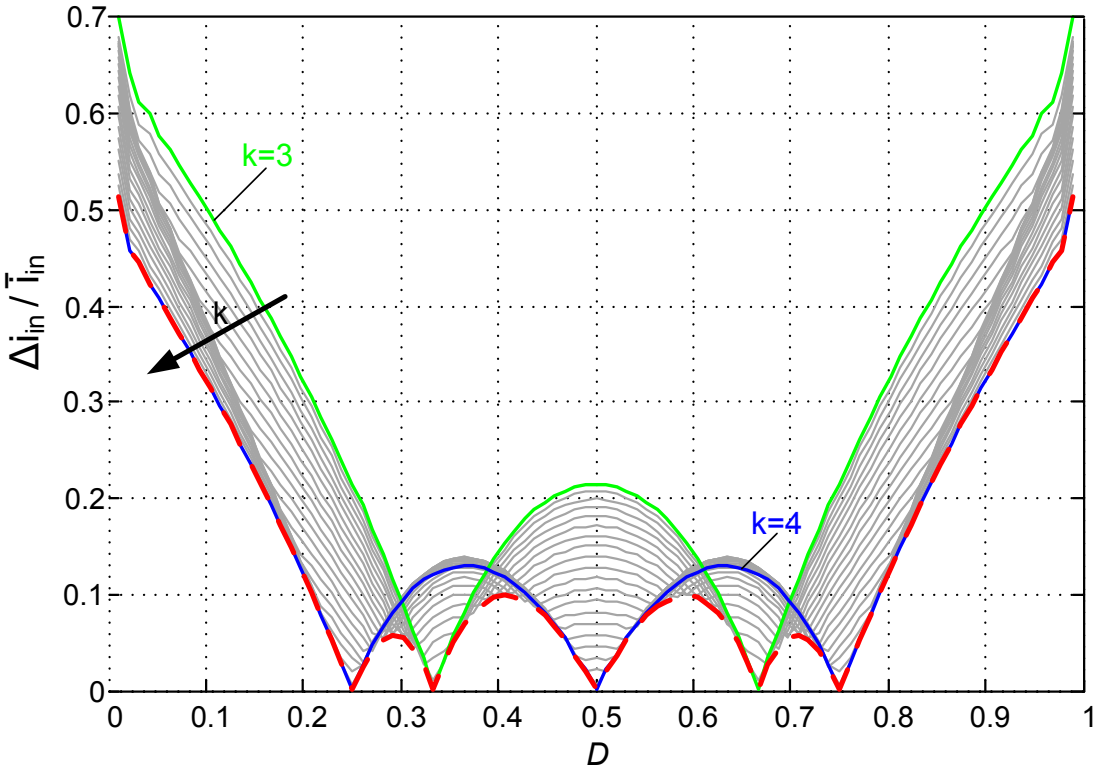

Fig. 2. Normalized input current ripple vs. duty ratio for $k = 3$ (green) and $k = 4$ (blue) interleaved phases, for fractional values $k = 3 \ldots 4$ (grey) with increments of $\Delta k = 0.05$ and minimum current ripple curve (dashed red)

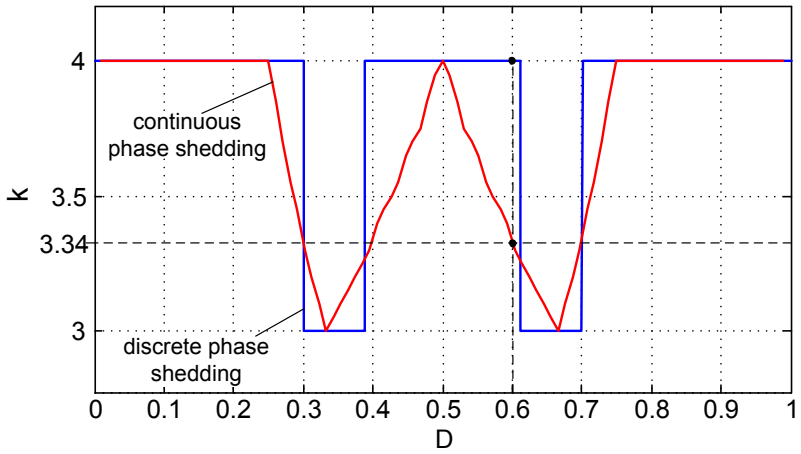

Fig. 3. Control law for minimum input current ripple with discrete phase shedding (blue) and with continuous phase shedding (red)

Note: If the duty ratio D is used for DCM, it represents the voltage ratio

$$D = \frac{V_{out} - V_{in}}{V_{out}} \tag{6}$$

and not the ratio of the on-time and the switching period.

Due to applying continuous phase shedding with fractional values of $k = 3 \ldots 4$ the resolution increases (cf. Fig. 2 grey curves).

Inspecting the curves with the minimum current ripple for each duty ratio it is obvious that in a wide duty ratio range the minimum ripple is further reduced due to the increased resolution of continuous phase shedding. A minimum ripple curve (Fig. 2 dashed red curve) can be extracted and the corresponding control law can be deduced (cf. Fig. 3 red curve).

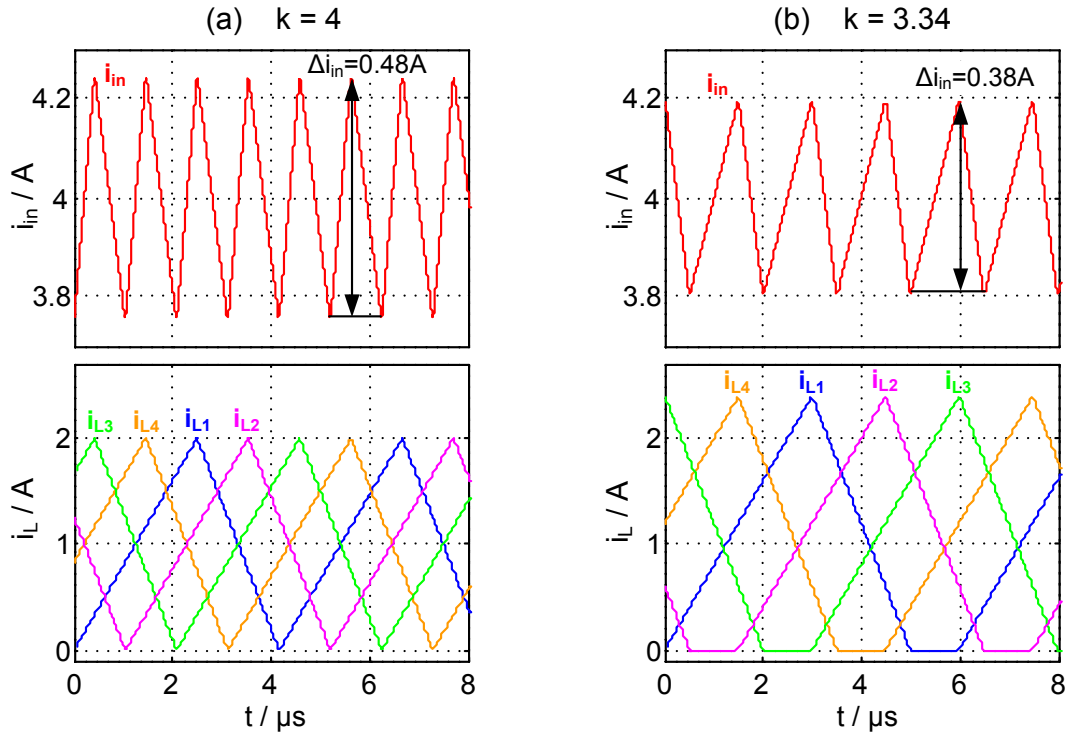

Fig. 4. Phase currents and resulting input current at $D = 0.6$ (a) without phase shedding ($k = 4$) and (b) with continuous phase shedding ($k = 3.34$)

Compared to the control law with discrete phase shedding there are no steps now. This is one basic requirement for applications with continuous varying duty ratio, e.g. PFC converter.

The benefit of this optimization compared to the un-optimized case becomes visible from the current shapes in Fig. 4. The phase currents and the resulting input current are illustrated for an exemplary duty ratio of $D = 0.6$ to verify the effectiveness of the developed control law.

In Fig. 4 (a) no phase shedding is applied so that all four phases are operating in BCM. By applying the control law the effective number of energized phases is set to $k = 3.34$ at $D = 0.6$ (cf. Fig. 3). Accordingly all phases get a DCM ratio of $K_{lag} = 1.2$. And even though the phase peak currents increase, the ripple of the input current reduces by 21%.

3.2. Switching Frequency and Current Limitation

It was shown that the input current ripple can be reduced significantly by applying continuous phase shedding. However, the phase peak currents grow with increased DCM ratio K_{lag}. On the other hand very high switching frequencies can occur in some operation points especially in PFC applications. Consequently the limits in the switching frequency and the maximum valid peak current needs also to be considered when the current ripple is minimized with continuous phase shedding. For this reason the range of K_{lag} needs to be limited. The minimum value of K_{lag} is given by the switching period for BCM $T_{s,BCM}$ and the maximum switching frequency $f_{s,max}$

$$K_{lag,min} = \frac{1}{\sqrt{f_{s,max}\, T_{s,BCM}}}. \tag{7}$$

The phase current average value $\bar{i}_L$ and the maximum allowable peak current $\hat{\imath}_{L,max}$ determine the maximum value of K_{lag} by

$$K_{lag,max} = \frac{\hat{\imath}_{L,max}}{2\,\bar{i}_L}. \tag{8}$$

With (7) and (8) the valid DCM ratio range is given by

$$\frac{1}{\sqrt{f_{s,max}\, T_{s,BCM}}} \leq K_{lag} \leq \frac{\hat{\imath}_{L,max}}{2\,\bar{i}_L}. \tag{9}$$

Expressing this operating range for the number of effective energized phases k, it follows

$$n \cdot \frac{2\,\bar{i}_L}{\hat{\imath}_{L,max}} \leq k \leq n \cdot \sqrt{f_{s,max}\, T_{s,BCM}}. \tag{10}$$

The dedicated borders $K_{lag} \geq 1$ and $k \leq n$ must still be maintained.

By reaching a limit it is obvious to operate the converter with this boundary value. But retaining this boundary value must not be the optimum valid value for the minimum current ripple. Strictly speaking the new optimal DCM ratio needs to be identified from the valid range. However, this could result in undesirable steps in the peak currents and switching frequency, for which reason an operation with the boundary value is the recommended way.

4. THD Minimization for Unequal Inductance Values

One major advantage of interleaving n converters with equal inductance values is the elimination of the first $n-1$ harmonics in the input current. The requirement is a time shift of T_s/n between the phase currents. But, if there is a variation in the inductance values this effect disappears and all harmonics are present. However, with adjusted phase shift values it is possible to reduce or even to eliminate the first harmonics.

If there is no restriction due to current balancing demand [3], the balancing factor K_b can be utilized to enable an individual DCM ratio for each phase. This degree of freedom can be utilized to eliminate further harmonics.

The formula to compute the Fourier coefficients is modified to

$$Q_\nu = \frac{\bar{i}_L\, K_{lag}^2}{2\pi^2 \nu^2 D(1-D)} \left[e^{-j\nu D \frac{K_b}{K_{lag}} 2\pi} - 1 + D - D\, e^{-j\nu \frac{K_b}{K_{lag}} 2\pi} \right]. \tag{11}$$

The validation of the optimizations is conducted with $n = 3$ parallel converters, but the methods can be easily modified for other numbers of interleaved phases. Inductance values with 5% deviation are applied for the exemplary calculations (cf. Table 1). Furthermore, the master phase with the largest inductance operates in BCM ($K_{lag} = 1$) and its average current is chosen to $i_{L1} = 1A$ for validations.

Table 1: Variation in the utilized inductance values

	inductance value	relative inductance
L_1	200 µH	100%
L_2	190 µH	95%
L_3	180 µH	90%

In order to eliminate harmonic components a system of equations needs to be set up. For each harmonic which should be eliminated the real and imaginary part must be set to zero. Hence, two independent variables are required to eliminate one harmonic component. These independent variables are the phase shift angles φ_i of the slave phases and the balancing factors K_{bi} which can give every slave phase an individual DCM ratio.

For $n = 3$ parallel phases two harmonic components can be eliminated. The phase shift angle of the master phase is fixed to zero and the remaining two phase shift angles can be modulated. The balancing factor of the master phase must be set to $K_{b1} = 1$ and the balancing factors of the slave phases can be randomized, if there is no current balancing restriction. In this case the system of equations to eliminate the 1st and 2nd harmonic in the input current can be expressed as

$$\begin{aligned} Re\{Q_{1,1}\} + Re\{Q_{2,1}\} + Re\{Q_{3,1}\} &= 0 \\ Im\{Q_{1,1}\} + Im\{Q_{2,1}\} + Im\{Q_{3,1}\} &= 0 \\ Re\{Q_{1,2}\} + Re\{Q_{2,2}\} + Re\{Q_{3,2}\} &= 0 \\ Im\{Q_{1,2}\} + Im\{Q_{2,2}\} + Im\{Q_{3,2}\} &= 0 \end{aligned}. \tag{12}$$

Where $Q_{i,\nu}$ represents the Fourier coefficient with the order ν of the current in phase i (cf. (11)).

Because the nonlinear system of equations cannot be solved in an analytical way, the numeric Newton method was utilized. With the Newton method, the phase shift angles and balancing factors for the entire duty ratio range were determined. The resulting curves are depicted in Fig. 5. It is striking that a discontinuity appears in the curves of the phase angles at $D = 0.5$. This means that the two slave phases needs to interchange their order to eliminate the 1st and 2nd harmonic. The curves of the balancing factors are continuously and have symmetry to the $D = 0.5$ axis.

In Fig. 6 the spectrum of the input current is given for $D = 0.6$. The corresponding phase and input current shapes are depicted in Fig. 7. In this figures also the situation without optimization are shown, i.e. default values $K_{b2} = K_{b3} = 1$, $\varphi_2 = 120°$ and $\varphi_3 = 240°$ are applied. By looking at the frequency spectrum without optimization in Fig. 6 the appearance of the 1st and 2nd harmonic can be seen. With optimized phase angles and balancing factors the 1st and 2nd harmonic are eliminated successfully. A reduction of the other harmonic components cannot

be guaranteed. Some components even get higher amplitudes. Due to this fact the reduction of the THD is not inherent. However, at most duty ratios an improvement of the THD is achieved, additionally.

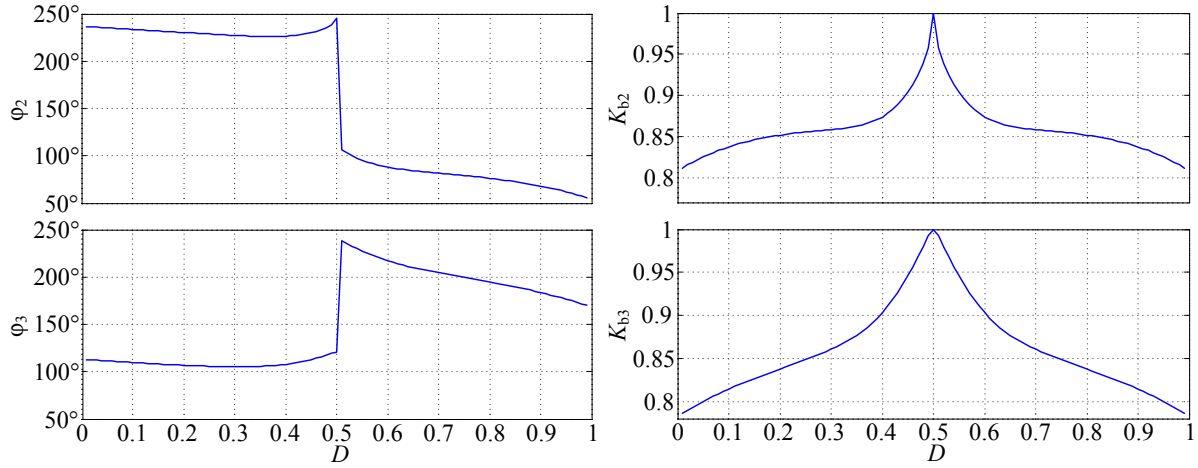

Fig. 5. Characteristic of the phase angles φ_2, φ_3 and the balancing factors K_{b2}, K_{b3} versus the duty ratio in order to eliminate the 1st and 2nd harmonic

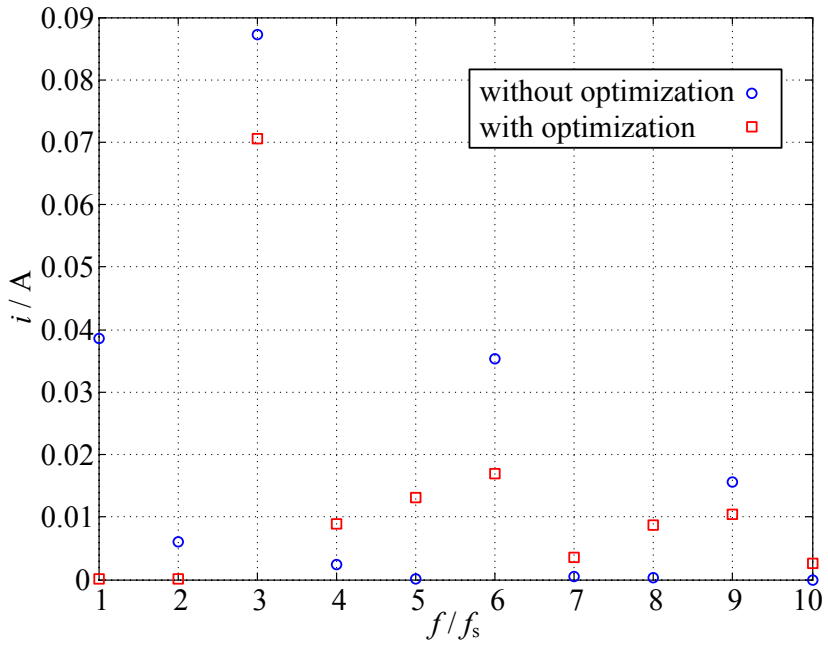

Fig. 6. Harmonic components with and without optimization at $D = 0.6$

The phase currents and the resulting input current are illustrated in Fig. 7 without DC component. All phases operate with individual DCM ratios and phase shifts in the optimized case. By looking at the input current it is distinguishable that with eliminating the first and second harmonic also the peak-to-peak current ripple is reduced, significantly.

For further THD reduction the optimal DCM ratio of the master phase can be identified like described in section 3.1. But this would enormously increase the computational effort. However, utilizing the universal control law for equal inductances is a good compromise.

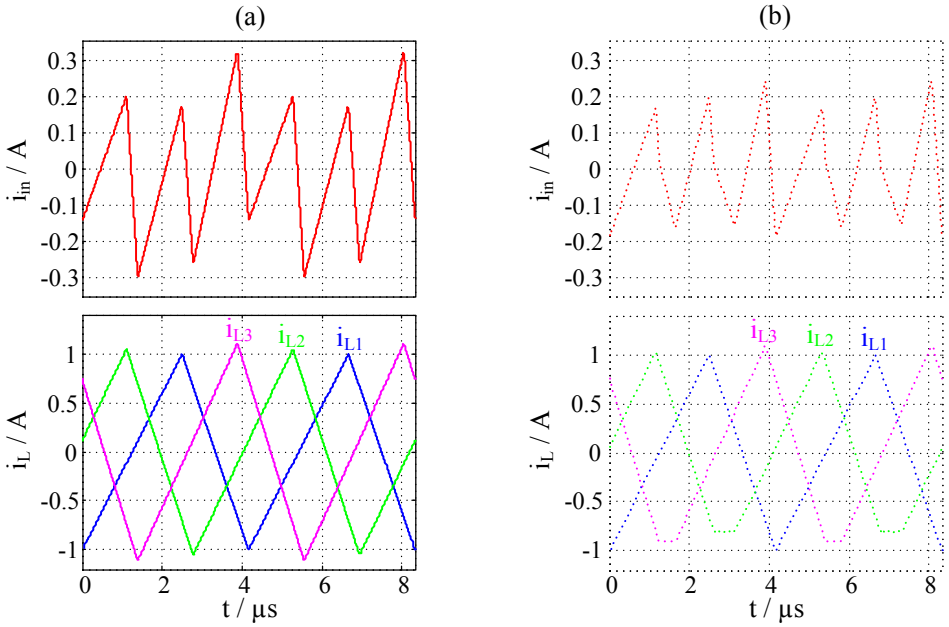

Fig. 7. Phase currents and resulting input current without DC component at $D = 0.6$ (a) without and (b) with optimization

5. Conclusion

With interleaving of several converters the first harmonic components are eliminated and the THD and the input current ripple are significantly reduced. In DCM further reduction can be attained by adjusting the DCM ratio. A universal control law can be generated for every number of paralleled phases to operate the converter with minimum THD and current ripple at any duty ratio.

If the inductance values are unequal, the first harmonics are no more eliminated by applying equal phase shift values. The optimal phase shifts needs to be computed depending on the inductance ratios for the entire duty ratio range. Additionally the balancing factor which gives every single phase an individual DCM ratio can be utilized to eliminate further harmonic components. The optimal values for the phase shifts and balancing factors are computed numerically with the Newton method. The computed values are only valid for the given inductance ratios and therefore need to be updated for each set of inductors. A generalized control law cannot be generated. The values for the optimal phase shift can change with steps at particular duty ratios. Accordingly, restrictions must be accepted so that an optimal elimination of harmonic components is not realizable in every application.

6. Literature

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