Cost-Effective Implementation of a Digitally Controlled LLC Resonant Converter for Application in Server- and Telecom-PSUs

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Abstract

The LLC resonant converter has become very popular for use in high efficient DC-DC converters in past years. Whereas the good efficiency of the LLC converter was demonstrated before, the design engineer is faced now with the problem of a cost-effective and reliable implementation of the LLC converter for the purpose of mass production and broad applicability. In this paper a cost-effective design variant is presented, which combines the digital control facilities of a low cost DSP and his peripheral PWM features with the critical control needs of the synchronous rectification (SR), thereby dealing with the parasitic effects that complicate turn-off instant sensing via R_{DSon} voltage drop of the rectifier MOSFETs. Additionally an adaptive voltage controlling approach is presented.

1. Introduction

Actual front-end rectifiers for server and telecom applications comprising the LLC converter are known to have best in class efficiencies of higher than 97% measured from 230V AC input to 54V DC output. But generally the LLC converter increases the circuit complexity as well as the control complexity of the DC-DC converter adding costs and affecting the performance of the output quantity control functions. In recent literature the extensive use of digital control methods is proposed [1-3] to tackle the challenges of increased circuit complexity of the LLC DC-DC converter in a cost effective and flexible way. In fact OEM prices of low-cost DSP solutions have become attractive and performance and peripheral features are strong enough to implement digital control structures into high performance industrial power supplies. The main obstacles of reliable LLC resonant converter design that can be solved in a cost effective way by means of digital implementation are:

- *Synchronous Rectification (SR) implementation*
  SR is a main issue of the LLC converter and discussed in numerous papers, e.g. [2-5].
- *Tight output voltage control throughout whole operating region*
  Output voltage control of the LLC converter is not intensively discussed in literature but becomes an issue when competing with the performance of traditional PWM control methods.
- *Light load operation, i.e. Burst Mode operation*
  Burst Mode operation for the LLC converter on the one hand is demanded from efficiency point of view and on the other hand can be used to cope with high input/output voltage ranges. Digital control methods help in obtaining the best burst mode operational performance [1,6].

Motivated by those facts this work demonstrates a highly digitized solution based on the Texas Instruments TMS320F28027 “Piccolo” DSP. The characteristic features of the chosen DSP are:

- 4 PWM units that can be synchronized to each other
- 2 integrated digitally adjustable analog comparators that can trip the PWM signals cycle by cycle
- 60 MHz 32 bit operational speed sufficient to control the LLC converter and perform all other tasks like supervision, system communication etc. in parallel
- low cost

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By utilizing these features a highly digitized control solution like shown in Fig. 1 can be realized. In this paper the SR implementation and the adaptive output voltage control are highlighted and measurement results on a prototype are presented. The contemplated application of the prototype is a Telecom- or Server-PSU with an extended output voltage range of e.g. 41 V – 58 V, which is typical in case of a direct battery backup of the output voltage. The rated output power of the prototype is 2500 W and the nominal switching frequency is 100 kHz.

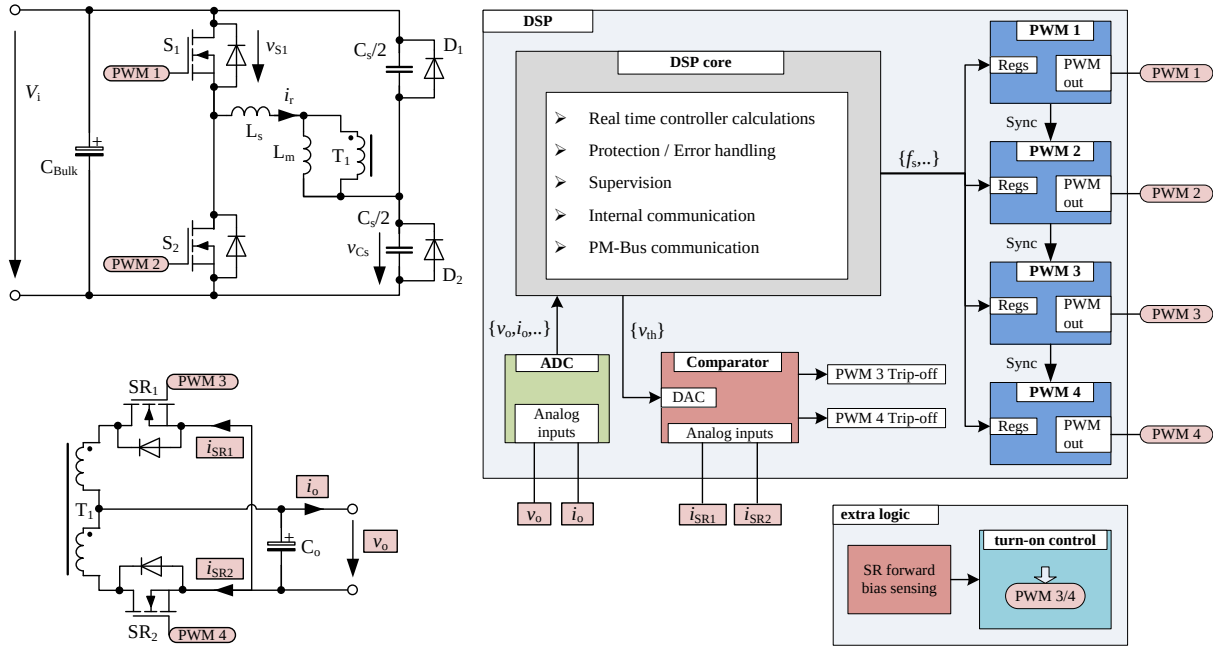

Figure 1: *Basic structure of the highly digitized control solution for LLC resonant converters*

2. Synchronous Rectification Requirements and Implementation

2.1. SR Control Requirements for the LLC Converter

Common SR control techniques for PWM converters are usually based on either directly deriving the SR gate signals from the inverter gate signals and/or from measuring some transformer voltage. These methods rely on the characteristic of most PWM converters that the appropriate conduction states of the rectifier MOSFETs (SR-FETs) coincide with the switching state of the inverter. Of further advantage is that the current commutation process within the rectifier stage introduces a small delay to the SR-FET conduction states that is good to account for the SR-FETs turn-on and turn-off delay times.

Disadvantageously this working principle is useful only for the continuous conduction mode (CCM), whereas in the discontinuous conduction mode (DCM) the SR gate signals must be disabled because at DCM the appropriate SR-FET conduction states no longer coincide with the switching state of the inverter bridge. However, for the LLC converter the appropriate SR-FET conduction states do not coincide with the switching state of the inverter bridge in almost the whole operating region due to the reactive nature and decoupling effect of the resonant circuit. Instead the rectifier switching state is, except at exact resonance point, phase shifted to the inverters switching state (c.f. Fig. 2 and 3). In consequence alternative SR gate driving signals must be applied for the LLC resonant converter.

The SR gating issue for resonant converters is addressed in many articles. Out of these and from fundamental considerations three basic principles utilized to derive SR gate drive signals can be summarized:

- Direct sensing of the rectifier current via current sense transformer
- Indirect sensing of the rectifier current via R_{DSon} voltage drop
- Sensing the body diode forward voltage drop which is normally much higher than the R_{DSon} voltage drop during channel conduction

Commonly the sensed signals are fed to a comparator to perform turn-on and turn-off decisions. A different but more complex approach is [3].

All those principles share the characteristic that they cannot be used to realize a so-called emulated ideal diode characteristic for the SR-FETs, because turn-on and turn-off delay times of actual FETs and drivers are typically too high to guarantee proper switching at all possible d*i*/d*t*-rates of the rectifier current. In consequence methods based on those principles must incorporate additional measures and/or logic to become reliable, safe and fault tolerant. Two main issues are essential and discussed in the following:

A first issue is that the rectifier current and the SR-FETs drain source voltages typically exhibit distinctive oscillations caused by stray inductances and semiconductor junction capacitances. The most distinctive oscillation occurs during the rectifier current discontinuity when the LLC converter operates in DCM as shown in Fig. 2. An analysis of this oscillation is given in Chapter 2.2. However, due to the distinctive nature of this oscillation it is necessary to ensure that no false turn-on decisions for the SR-FETs are made. Due to the turn-on and turn-off inertia of the SR-FET switching, false turn-on decisions would disturb converter operation and chaotic waveforms may result. Omitting this can be achieved by two measures:

- Using the switching state of the inverter to inhibit resp. release the SR-FET turn-on triggering omits false turn-on caused by the oscillation prior normal turn-on (c.f. Fig. 2).
- To omit false turn-on caused by the oscillation after normal turn-off a state machine like approach can be used: The SR-FET should be only able to turn-on once per switching period.

Both measures are implemented by appropriate configuration of the PWM units within the DSP (c.f. Fig. 1). It should be noted here that the internal synchronisation between the inverter PWMs (PWM1, PWM2) and the SR PWMs (PWM3, PWM4) is an essential function for the proposed solution.

A second issue is that the resonant current exhibits high d*i*/d*t*-rates at the end of the SR-FETs conduction period when the LLC converter operates at above resonance (CCM, c.f. Fig. 3). Practical experience shows that it is difficult to deal with those high d*i*/d*t*-rates due to unavoidable delay times within the SR processing circuitry (e.g. ~100 – 200 ns). Thus a common but nevertheless non optimal workaround here is to simply retain the solution of issues 1, i.e. utilizing the inverter switching state as an inhibit resp. release signal, as well for the above resonance (CCM) operation. By doing so the resp. SR-FET is turned off prior to the high d*i*/d*t*-rate section of the resonant current, resulting in additional body diode conduction time but guarantying safe SR-FET turn-off for all load conditions.

Whereas the need for solving issue 2 depends on the speed capabilities of the SR processing circuitry, the DSP PWM units can also be configured to extend the Release signal for some amount of time (c.f. top of Fig. 3), so that the SR-FET turn-on time can also be extended if desired and SR processing circuitry is capable of the high d*i*/d*t*-rates. Another feature of the DSP PWM solution is that a signal to realize a minimum-on-time (MOT) can be supplied and tuned dynamically.

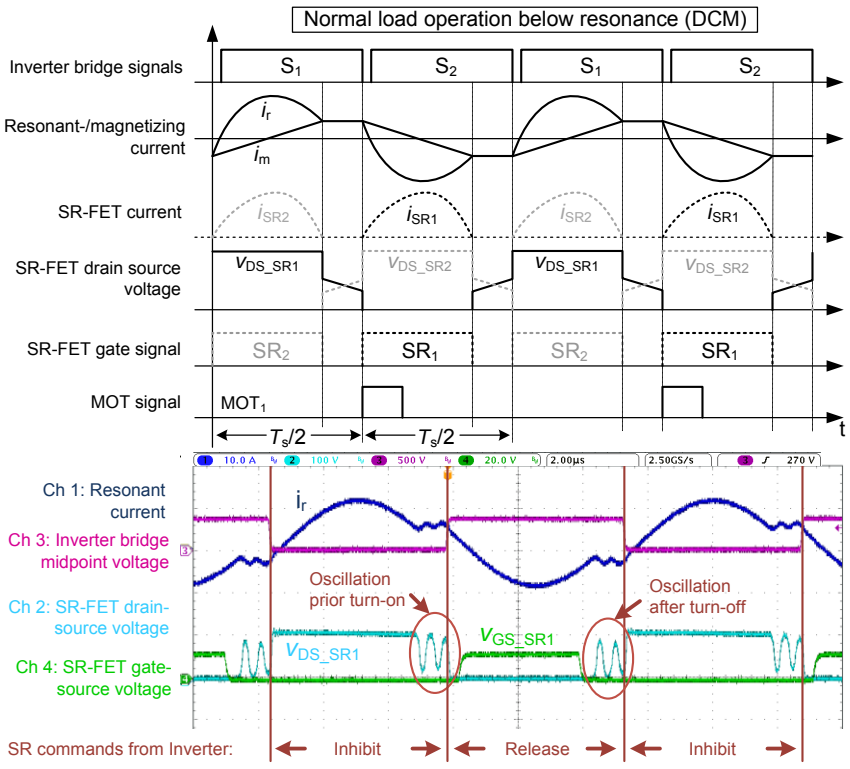

Figure 2: *Principle and measured waveforms of a LLC converter at below resonance operation and normal load conditions*

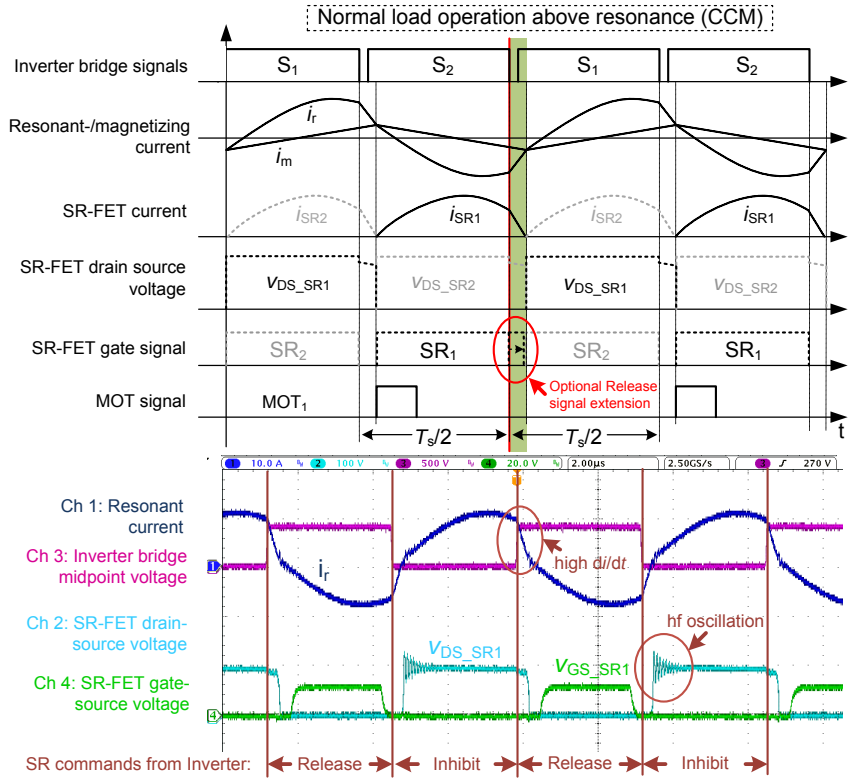

Figure 3: *Principle and measured waveforms of a LLC converter at above resonance operation and normal load conditions*

2.2. Analysis of Rectifier Voltage Oscillations

As stated in Chapter 2.1 the real LLC converter exhibits additional oscillations caused by XFMR stray inductances and semiconductor junction capacitances. To identify the parasitic resonant circuits the equivalent circuit shown in Fig. 4 can be used [7]. The equivalent circuit is valid for the center-tapped as well as for the full-wave rectifier type.

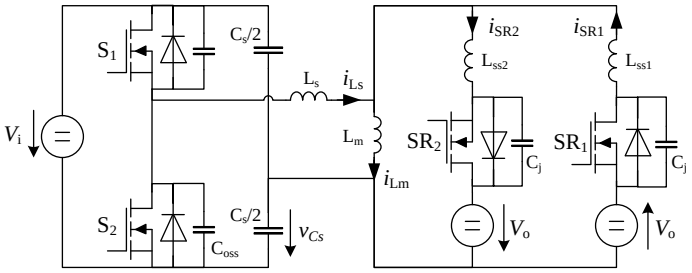

Figure 4: *LLC converter equivalent circuit with XFMR unity turns ratio assumed*

The oscillation path that is active during the output current discontinuity in DCM mode (see Fig. 2) is shown in Fig. 5-A. The involved resonant elements are the resonant inductor L_s and the junction capacitances C_j of the rectifier switches. Thus the resonant frequency is given by

$$f_{0\_par1} = \frac{1}{2\pi\sqrt{(L_s + \frac{1}{2}L_{ss})2C_j}}$$

Because the resonant inductor L_s is involved in this oscillation, the resonant frequency is quite low and little damped. The excitation of the resonance depends on the actual load condition, i.e. the actual voltage of the resonant capacitor C_s, and thus cannot be freely influenced by design. Minimizing the rectifier junction capacitances C_j increases the resonant frequency but has no effect on the resonance amplitude or excitation. In consequence there is a general risk of disturbed SR operation by this oscillation and aforementioned measures as described in Chapter 2.1 are evident for reliable SR operation at all load conditions.

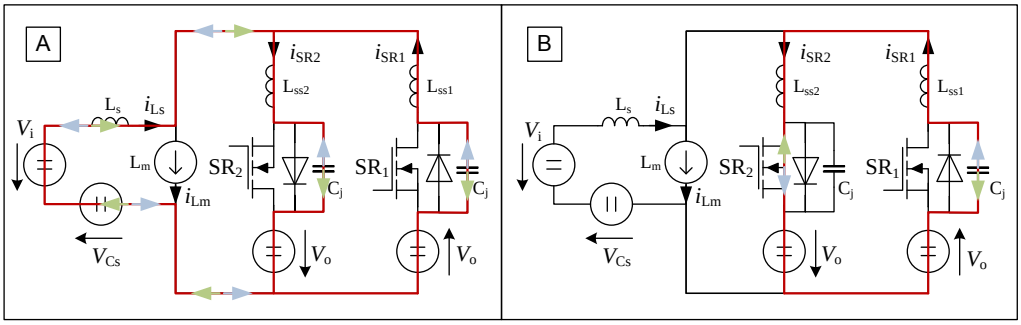

Figure 5: *Equivalent circuits showing parasitic resonant circuit paths*

A second oscillation path is shown in Fig. 5-B. It is formed by the junction capacitances C_j of the reverse biased rectification leg and the stray inductances L_{ss1} and L_{ss2} of the respective rectifier current paths. Because the stray inductances are usually kept small by design, the resonant frequency here is quite high and distinctively damped (see Fig. 3). It is given by

$$f_{0\_par2} = \frac{1}{2\pi\sqrt{2L_{ss}C_j}}$$

The excitation of this oscillation depends on two main factors: The first one is the amount of leakage inductance L_{ss}; the more leakage inductance the higher the excitation. The second one is the reverse bias characteristic of the body diode; the more reverse recovery charge the higher the leakage inductance loading and thus the excitation. Due to the recovery characteristic involved in this oscillation, the excitation becomes clearly load dependent if the SR-FET is turned off prior to the high d*i*/d*t*-rate section of the resonant current according to the workaround described in Chapter 2.1; the higher the load the higher the reverse recovery charge of the body diode. The second oscillation (f_{0_par2}) typically affects the SR operation in

a way that the SR-FETs are turned off in direct succession to the turn-on. For this reason usually a minimum-on-time (MOT) configuration for the SR gate drive signals is applied.

For the sake of simplicity the above analysis neglects the coupling between oscillation path A and B. However, if stray inductances L_{ss} are kept small compared to resonant inductance L_s, the coupling is quite small. In the real world a fourth order system results in case of both rectification legs are reverse biased (Fig. 5-A) and a third order system in case of one rectification leg conducting (Fig. 5-B). Thus exact analysis would be much more involved but give little relevant details.

2.3. Discussion of Rectifier Conduction State Sensing Methods

The proposed highly digitized control solution (c.f. also Fig. 6) is flexible with respect to the sensing methods applied for determining the SR-FET conduction state. Basically the sensing method can be different for turn-on and turn-off instances. Known methods for the turn-on instant are to compare the SR-FET forward current or to compare the SR-FET body diode forward voltage to a turn-on threshold. The turn-on instant is not critical, because delayed turn-on only adds to the body diode conduction time. The only known method for the turn-off instant is to compare the SR-FET forward current to a turn-off threshold. The turn-off instant is critical, because delayed turn-off results in a reverse current which increases switching losses and in a worst case destroys the SR-FET.

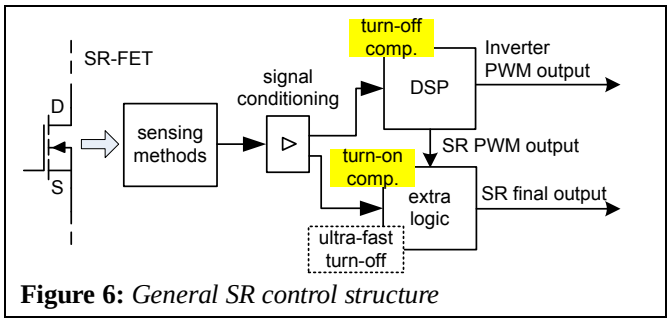

Figure 6: *General SR control structure*

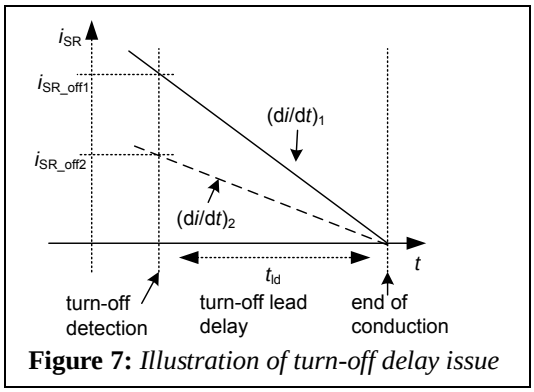

Figure 7: *Illustration of turn-off delay issue*

Turning off the SR-FET in time is complicated by delay times within the turn-off processing circuitry that add to the overall turn-off delay t_{off}. Delays are e.g. the comparator, logic gates, drivers and the SR-FET itself. In consequence the turn-off detection must lead the SR-FETs end of conduction by the turn-off lead delay t_{ld} as illustrated in Fig. 7. Optimal turn-off switching results if $t_{ld} = t_{off}$ is met. Because the di/dt current slope varies with different load conditions the optimal turn-off threshold i_{SR_off} varies as well. One solution is to adapt the turn-off threshold with load, which can be easily implemented within the DSP (c.f. Fig. 1). However, besides higher complexity dynamic adaptation of the turn-off threshold is risky when fast load changes occur, e.g. in case of a load step. Another solution is to implement ultra-fast turn-off, at which the turn-off delay t_{off} is minimized by somehow direct coupling of the SR-FET current sensing XFMR with the SR-FET gate driver. This solution would be only reliable when using the full-wave rectifier type, because in case of the center-tapped rectifier type two current sense XFMRs are needed and each adds parasitic inductance to the commutation loop.

From above discussion a solution is proposed especially for applying the center-tapped type rectifier, which has the advantage that no high-side driving for SR-FETs is required. The solution is based on indirect sensing of the rectifier current by sensing the R_{DSon} voltage drop of the SR-FETs. This method is commonly utilized by discrete SR driving ICs like [8]. It unfortunately suffers from the presence of package inductances which distort the R_{DSon} voltage drop measurement. Workarounds that try to compensate the inductive voltage drop by measuring the di/dt current slope [8] or by adding RC compensation networks [5] are of higher effort.

The proposed solution relies on the effect that the inductive voltage drop can cancel out with the need for adapting the turn-off threshold with load, if values are tuned well.

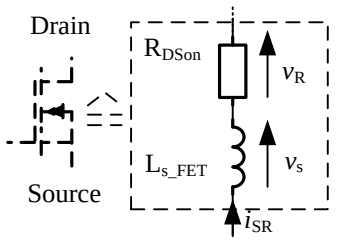

Figure 8: *Equivalent circuit of conducting MOSFET*

According to Fig. 8 the R_{DSon} voltage drop v_R and the inductive voltage drop v_s superimpose to the sensed source-drain voltage $v_{SD} = v_R + v_s$, which is given by

$$v_{SD} = R_{DSon} i_{SR} + L_{s\_FET} \frac{di_{SR}}{dt}$$

Assuming that the current slope is linear, which is a well approximation for sinusoidal shapes in the vicinity of the zero crossing, the optimal turn-off detection threshold current $i_{SR} = i_{SR\_off}$ is given by

$$i_{SR\_off} = -\frac{di_{SR}}{dt} t_{off}$$

Thus the sensed voltage at the optimal turn-off detection instant is given by

$$v_{SD}@i_{SR\_off} = -R_{DSon} i_{SR\_off} + L_{s\_FET} \frac{di_{SR}}{dt}\Big|_{i_{SR\_off}}$$

$$= (-R_{DSon} t_{off} + L_{s\_FET}) \frac{di_{SR}}{dt}\Big|_{i_{SR\_off}}$$

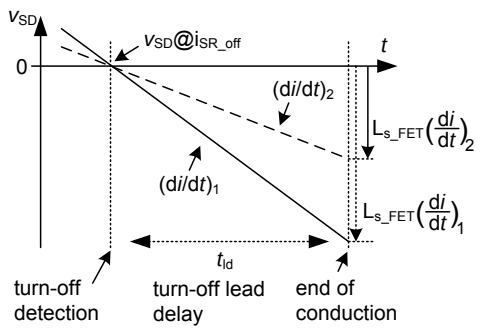

Figure 9: Sensed voltage v_{SD} prior end of conduction

From these basic equations it is clear that the optimal turn-off threshold voltage becomes independent of the actual current slope if $R_{DSon} t_{off} = L_{s\_FET}$ is met, i.e. the optimal turn-off threshold $v_{SD}@i_{SR\_off}$ becomes zero (c.f. Fig. 9). In order to utilize this characteristic the dimensions of each factor R_{DSon}, t_{off} and L_{s_FET} must be suitable. As an example the IPB072N15N3 has ~5 nH package inductance (TO263) and on-resistance at 60°C is 7.5 mΩ. This results in a turn-off delay of t_{off} = 667 ns, which for e.g. 100 kHz resonance frequency is app. 1/10th of half the resonance period and thus is still acceptable considering the deviation of the sinusoidal current slope from the assumed linearity.

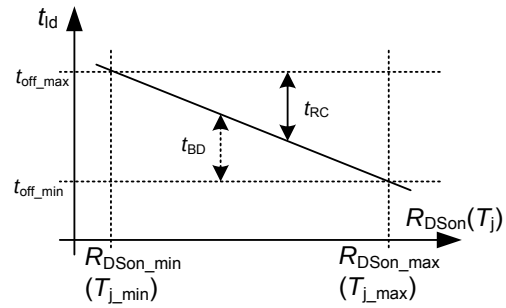

Figure 10: *Turn-off lead delay vs. on-resistance*

Unfortunately the on-resistance varies with temperature, so that $t_{ld} = t_{ld}(T_j)$. In consequence either the turn-off delay t_{off} has to be adapted with temperature, or imprecise turn-off has to be accepted. For simple implementation the latter is chosen here, but some considerations are necessary (c.f. Fig. 10): In order to prevent reverse currents the turn-off delay t_{off} has to be chosen for the maximal expected junction temperature T_{j_max} of the SR-FETs, i.e. $t_{off} = t_{off\_min}$. Therefore at lower junction temperatures a body diode conduction time $t_{BD} = t_{ld} - t_{off\_min}$ has to be accepted. If the turn-off delay t_{off} would have been chosen for not the maximal junction temperature, e.g. $t_{off} = t_{off\_max}$, a reverse current time $t_{RC} = t_{off\_max} - t_{ld}$ would occur in case of higher junction temperatures, which must be avoided for reliable operation.

In case of the IPB072N15N3 example a maximum junction temperature of 110°C is assumed which results in 10 mΩ on-resistance and in a lead delay of $t_{ld@110°C}$ = 500 ns, which should

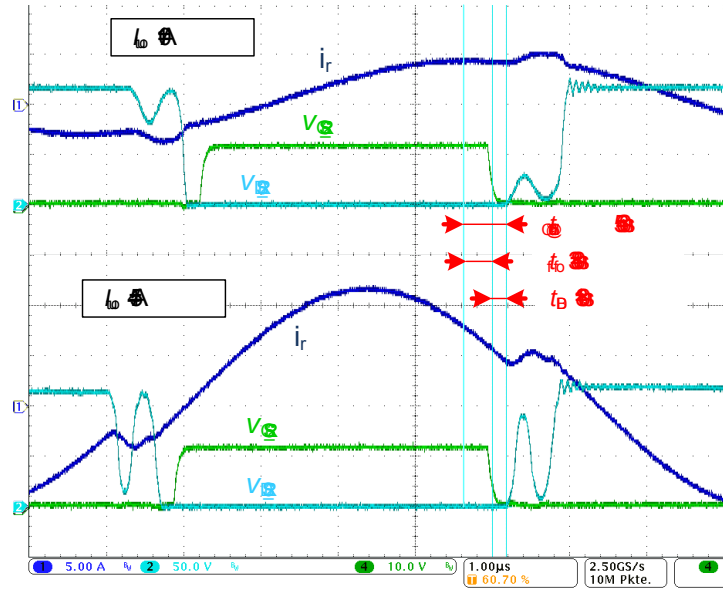

Figure 11: *Prototype measurement of SR performance with optimal tuned turn-off threshold voltage and turn-off delay time at normal junction temperature (~50°C)*

be set for the turn-off delay, i.e. $t_{off} = t_{off\_min}$. In this case the body diode conduction time at $T_j = 60°C$ becomes $t_{BD} = t_{ld@60°C} - t_{off\_min}$ = 667ns – 500 ns = 167 ns, which is still acceptable from efficiency point of view. It is evident here that this t_{BD} is load independent without the need of adapting the turn-off threshold with load.

In prototype tests the load independent SR operation point was found to be at $t_{ld@50°C}$ = 560 ns (c.f. Fig. 11). The turn-off delay time is digitally fine-tuned within the DSP to become $t_{off} = t_{off\_min}$ = 380 ns, so that a body diode conduction time of t_{BD} = 180 ns results that shall account for up to the maximal expected junction temperature accordingly. The final t_{off} value should be confirmed by maximum temperature tests.

3. Adaptive Output Voltage Control

Fig. 12 shows in the left the measured control to output transfer behaviour of the LLC conver-

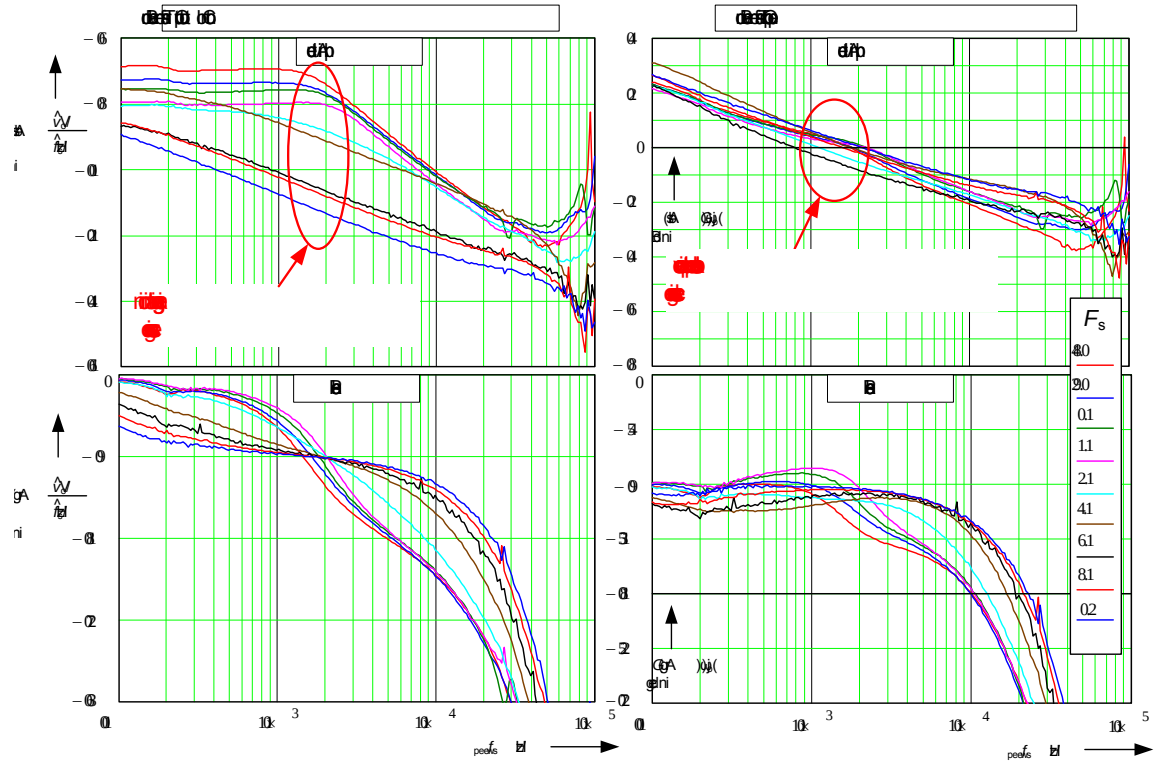

Figure 12: Left: Measured aviour; Right: C m-
pensation applied; V_i = con F_s: normalized

ter prototype, whereat the switching frequency f_s is the manipulated variable and the output voltage v_o the controlled variable. It can be seen that the compensator design is challenging due to the huge gain variation in the aimed cross over region for different switching frequencies. To cope with this characteristic an adaptive PID-compensator was programmed resulting in the open loop transfer behaviour shown in the right of Fig. 12, whereby a very close cross over region and quite unity transfer characteristics are achieved. A further problem arises due to the fixed point arithmetic of the used DSP; it is difficult in case of huge gain adaptations to compromise between calculation accuracy and over flow boundaries of the variables. However, this task was solved by using adaptive scaling for the compensator calculation, whereat the adapted compensator parameters are calculated offline resulting in a floating point like approach, and afterwards stored in a look-up table within the DSP memory. In operation the compensator parameters are read from this look-up table at every calculation cycle of the compensator according to the actual switching frequency f_s.

4. Conclusion

The digital control and peripheral features of available low cost DSP solutions enable the cost-effective implementation of the LLC resonant converter for use in Server- and Telecom-PSUs with wide input-/output voltage range. By utilizing the DSP PWM units to generate gating signals for the synchronous rectification a safe and reliable operation of the LLC converter can be achieved for all load conditions. In case of the high efficiency 54 V output prototype the ratio between package inductance and on-resistance of the used synchronous rectifier MOSFETs is suitable to employ the proposed turn-off instant sensing method, which makes use of the SR-FET package inductance to achieve a load independent turn-off threshold voltage. Furthermore, the adaptive controlling approach ensures stable and tight output voltage control throughout the whole operating region.

5. Literature

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