Full Digital Implementation of an Optimized Modulation Strategy for Series-Parallel Resonant Converter

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Abstract

The series-parallel resonant converter is one of the most popular topologies among resonant converters. In order to minimize its switching losses, an optimized modulation strategy was proposed and implemented using a hybrid hardware structure. In this contribution the working principles of the state-of-the-art hybrid solution and its disadvantages are analyzed first. In order to overcome those drawbacks, a full digital optimized modulation control unit is developed. Aiming to ensure zero-voltage switching in the converter start-up phase, a novel operation strategy is proposed and implemented. Experimental results are given to prove the feasibility of the novel digital optimized modulation control unit.

1. Introduction

Due to the zero-voltage switching (ZVS) character and the ability of utilizing parasitics, an increasing interest in resonantly operated DC-DC converters in super-resonant operation mode has been shown since it was introduced in the 1980s. Among the most applied two- and three-element resonant converters, the series-parallel resonant converter (SPRC) (Fig. 1.a) is one of the most popular converter topologies because it takes on the desirable characteristics of the series resonant converter (SRC) and the parallel resonant converter (PRC), while removing their main disadvantages [1].

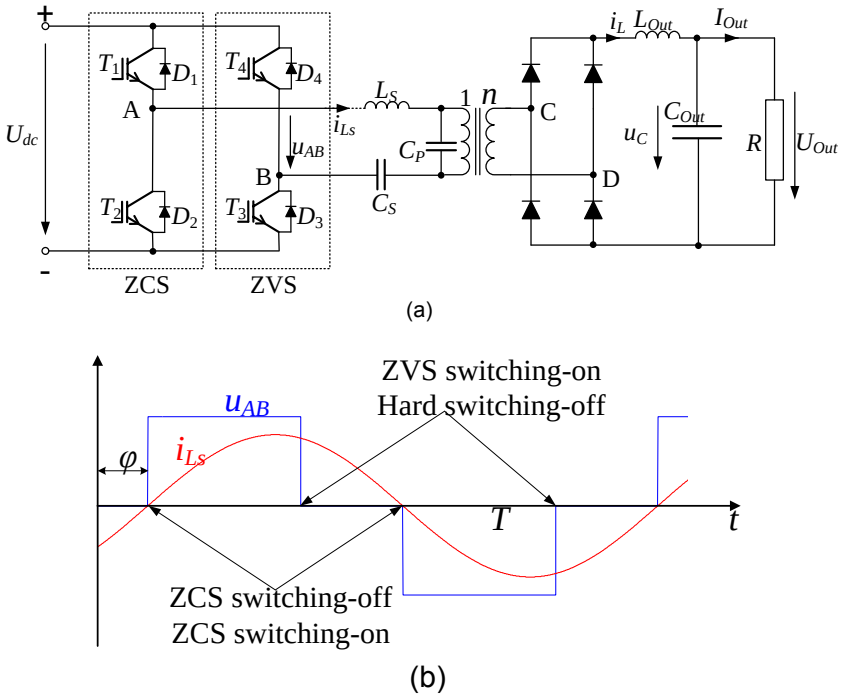


Fig. 1. (a) Circuit diagram of SPRC and (b) its current and voltage waveforms under optimized modulation

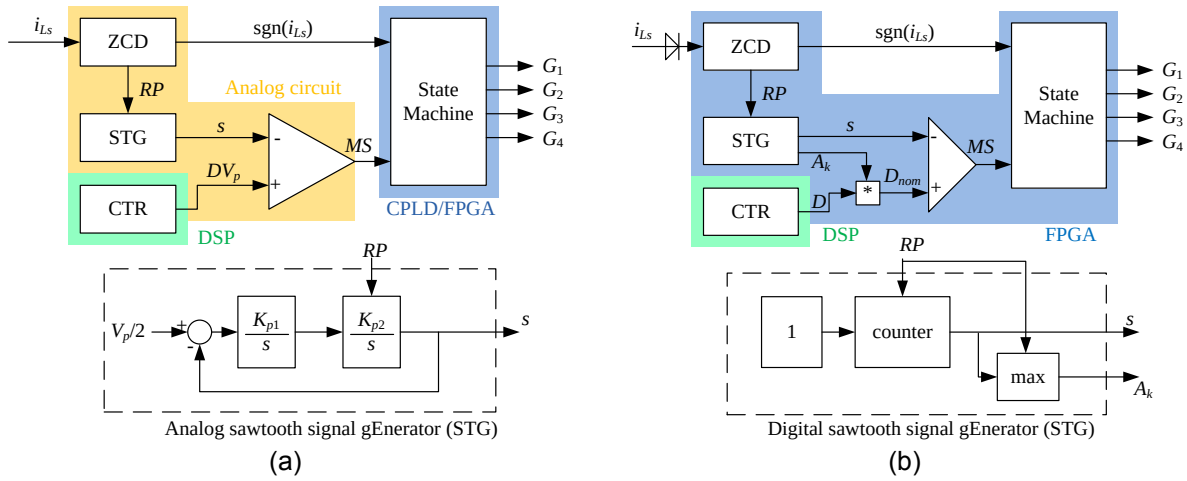


Fig. 2. Block diagram of (a) a hybrid and (b) a full digital OM control unit

Different from converters with pulse width modulation (PWM) the output voltage of a SPRC is usually regulated by switching frequency while keeping the duty cycle by one, which is called *standard modulation* (SM) in this paper. In order to achieve a further switching loss reduction, a novel modulation strategy combining switching frequency and phase-shifted controls, which is called *optimized modulation* (OM) in this paper, was developed and implemented by Pinheiro [2]. Under OM zero current switching (ZCS) is achieved on one full bridge leg and ZVS is achieved on another leg (Fig. 1.b). Hence, the only dominant switching loss is the turn-off loss of the ZVS leg. Comparison results show that the steady-state and dynamical characteristics of SRPC are strongly improved by using OM. However, its control complexity is much higher than SM [3].

The state-of-the-art technique to implement the OM strategy is to use a hybrid hardware structure containing an analogy circuit and a high speed programmable digital device. Its working principle and drawbacks are given in Section 2. In order to overcome those drawbacks, a novel full digital OM control unit is proposed in Section 3. Experiment results and the final conclusion are given in Section 4 and Section 5, respectively.

2. State-of-the-Art Hybrid Solution

As shown in Fig. 2a, the state-of-the-art hybrid OM control unit consists of an analog part and a digital part. Inputs of the analog part are the duty cycle DV_p ($0 < D < 1$) and the measured resonant current i_{Ls}. Its outputs are transistor gate signals. The control process begins with the resonant current zero-crossing detection block (ZCD), which monitors i_{Ls} and outputs a current direction signal sgn(i_{Ls}) and a reset pulse (*RP*) at current zero-crossing time instant. In parallel a sawtooth signal *s* with the amplitude V_p is approximated by an analog sawtooth signal generator (STG) and reset by *RP* at each current zero-crossing. Hence, *s* is synchronized with the resonant current and has a doubled resonant current frequency ($f_{Saw} = 2f_i$ and $T_{Saw} = 0.5T_i$). An analog comparator compares the sawtooth signal *s* to the duty cycle DV_p and outputs a modulation signal *MS*. Both Boolean signals sgn(i_{Ls}) and the *MS* are outputs of the analog part and inputs of the digital part. By means of a state machine, both Boolean signals are processed and the final transistor gate signals G1 to G4 are generated. In order to achieve a very high resolution, the state machine is required to be implemented on a very high speed programmable digital device, e.g. a field-programmable gate array (FPGA) or a complex programmable logic device (CPLD) [4] [5].

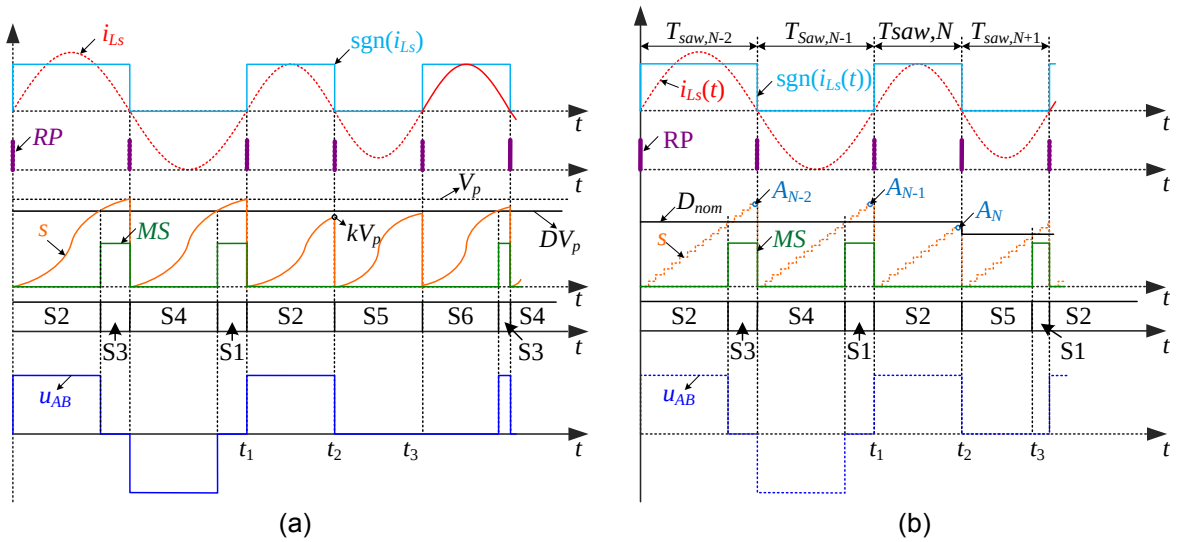


Fig. 3. Waveforms of the resonant current, inverter output voltage and signal of (a) a hybrid and (b) a full digital OM control unit

The waveforms of the resonant current, the inverter output voltage and signals of the hybrid OM control unit are illustrated in Fig. 3a. The state machine and its event table are given in Fig. 4. The converter has three operation modes: normal mode, protection mode and start-up mode. As shown in Fig. 3a, in steady-state operation ($t < t_1$) the SAW signal has a quasi-constant rated amplitude V_p and the state changes via the normal transition: S1 → S2 → S3 → S4. If a load step (from heavy load to light load condition) occurs at the time instant t_1, the SAW signal is reset before it reaches the rated amplitude *Vp*, e.g. reset at an amplitude of $s(t_1) = kVp$ (Fig. 3a at time instant t_2). If $k < D$, the modulation signal *MS* cannot be set and the converter goes into the protection state S5 (Fig. 4). The converter changes between ~~the~~ both protection states S5 and S6 at each current zero-crossing, until the next rising edge of the modulation signal *MS* appears. The duration of the protection states depends on the operation point and the dynamic character of the analog sawtooth signal generator. Thanks to both protection states, the ZVS condition is ensured for the ZVS-leg transistors both under steady-state operation and on transient [4] [5].

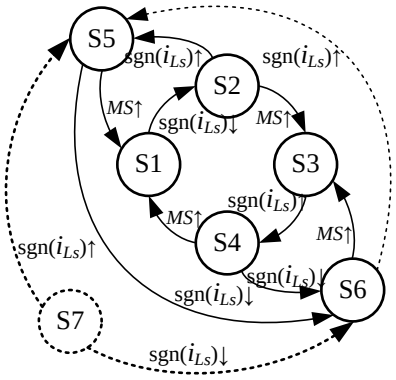
Major disadvantages of this solution are the very limited flexibility and signal processing capability (e.g. digital filtering, compensation of measurement delays, etc.), which are very important in practical application. Another drawback is that a tradeoff between the distortion in the sawtooth waveform and the dynamics of the sawtooth signal generator has to be done, which results for a sub-optimized sawtooth signal [5].

3. Full Digital OM Control Unit

3.1. Operation Principle

In a full digital OM control unit the current zero-crossing detection block, the sawtooth signal generator, the comparator and the state machine are implemented digitally within a single FPGA chip (Fig. 2.b). Current direction signal sgn(i_{Ls}) and reset pulse are generated using a digital comparator of the current zero-crossing detection block. The sawtooth signal *s* is generated by a digital counter and reset by RP. Hence, it has a constant slope and a variable amplitude. At the beginning of a period $T_{Saw,N}$ the duty cycle D ($0 < D < 1$) is normalized to the sawtooth signal amplitude A_{N-1} in the last period $T_{Saw,N-1}$ (Fig. 3.b)

$$D_{Nom}(t) = DA_{N-1}, \quad \text{for the period } T_{saw,N} \ (t_1 < t < t_2).$$



State	T_1	T_2	T_3	T_4	Sgn(i_{Ls})	*MS*
S1	ON	OFF	OFF	ON	-	-
S2	OFF	ON	OFF	ON	-	-
S3	OFF	ON	ON	OFF	-	-
S4	ON	OFF	ON	OFF	-	-
S5	ON	OFF	OFF	OFF	-	-
S6	OFF	ON	OFF	OFF	-	-
S7	OFF	OFF	OFF	OFF	true	false

Fig. 4. State-of-the-art and its event table of the OM control unit

The *MS* signal is set via comparing the normalized duty cycle D_{Nom} to the sawtooth signal *s* and reset by *RP*. Since the normalized duty cycle D_{Nom} is directly calculated by the sawtooth signal amplitude in the period, its response to frequency variation of a resonant current is very high. Thanks to the very high operation frequency and the parallel processing capacity of the FPGA technique, a distortion of the sawtooth signal is almost eliminated and very high duty cycle resolution is realized (e.g. 10 ns resolution at 100 MHz operation frequency). As profit from the full digital structure, a much better design flexibility is achieved and several useful functional blocks are implemented.

3.2. Compensation of Time Delays

For the practical application of the proposed OM control unit, three major time delays shall be compensated: the time delay of the measurement circuit (T_{d1}), the dead time of the inverter (T_{d2}) and the rising time of the transistor Gate-Emitter voltage (T_{d3}). As shown in Fig. 5a, if those time delays are not compensated, the turn-off action of T1 and the turn-on action of T2 occur after the current zero-crossing. That means that both switching actions occur under hard switching condition.

These time delays can be compensated by introducing an additional normalized duty cycle D_1 ($0 < D_1 < 1$), which is normalized to the sawtooth signal amplitude in the last period, too

$$D_{1Nom}(t) = A_{N\text{-}1}, \quad \text{for the period } T_{saw,N}.$$

As shown in Fig. 5b, under normal steady-state operation mode the sawtooth signal *s* reaches D_{1Nom} before the current zero-crossing and the current direction signal sgn(i_{Ls}) is directly set (or reset) at the time instant $s = D_{1nom}$. Under an ideal boundary condition ($D_{1nom} = D_{1nom,bou}$) all time delays are completely compensated ($T_{cp} = T_{cp,bou} = T_d$) and the transistor becomes conductive just at the current zero-crossing time instant (Fig. 5b). Since the time delays T_{d1} and T_{d3} are operation-point-dependent, the required steady-state boundary compensation time $T_{cp,bou}$ at different operation points are also very different. The maximum required boundary compensation time $T_{cp,bou,max}$ of the whole operation range is only experimentally deducible. In practical application, the compensation time T_{cp} is designed slightly longer than $T_{cp,bou,max}$, so that the commutation is completed shortly before the current zero-crossing. That means that transistors of the ZCS-leg have to switch off a very small current in hard-switching condition and turn on under ZVS condition. Using this compensation strategy, switching losses of the ZCS-leg are minimized for steady-state operation. In transients this compensation strategy does not ensure optimized switching timing of the ZCS-leg. However, a sub-optimized transient switching condition does not damage the overall efficiency of the converter.

Since D_{1nom} is normalized to the sawtooth signal amplitude in the last period, the following two situations can occur during transients:

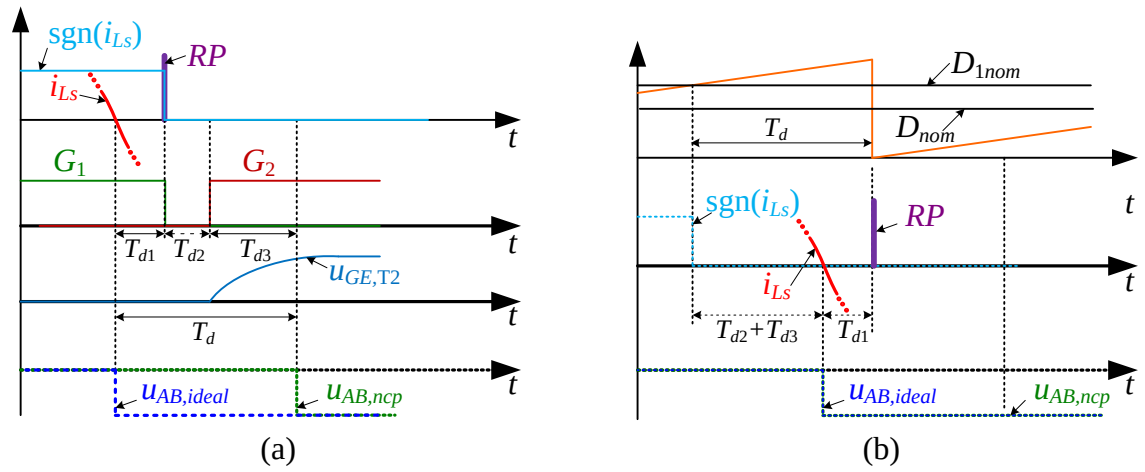


Fig. 5. Waveforms (a) without and (b) with compensation of time delays

- D_{1nom} is not available in the first period of the start-up phase
- The sawtooth signal s does not reach D_{1nom} at the current zero-crossing time instant

In both situations the compensation function is deactivated and the current direction signal sgn(i_{Ls}) is set/reset directly by the current zero-crossing.

3.3. Special Operation Mode for Start-Up Phase

In order to reduce turn-off the losses of the transistors of the ZVS-leg, capacitive snubbers are usually required. However, a capacitive snubber can only be applied if the ZVS condition is ensured in all operation modes. As discussed in Section 2, under steady-state operation and during transients, the ZVS is ensured through introduction of the protection states S5 and S6. In the start-up phase, a special operation mode is required, because the snubber capacitors are pre-charged by the DC-link voltage to a value $U_{dc}/2$. In order to describe the inverter blocking state, an additional state S7 is introduced (Fig. 4 dashed line). In this state, the *MS* is set to "false" and sgn(i_{Ls}) is set to "true".

The working principle of the start-up operation is illustrated in Fig. 6. Before the time instant t_0 the converter enable signal *En* is "false" and the converter is in state S7. At the time instant t_0 the enable signal *En* is set. After a short delay, which is implemented by a timer, sgn(i_{Ls}) is reset at the time instant t_1. The falling edge of sgn(i_{Ls}) changes the converter state from S7 to S6 and turns on transistor T2. During the time interval $t_1 < t < t_2$ the upper snubber capacitor C_U is charged and the lower snubber capacitor C_D is discharged. At the time instant t_2 C_D is completely discharged and the diode D3 becomes conductive. The current flows via T2 and D3. Since the normalized duty cycle signals D_{nom} and D_{1nom} are not available yet, sgn(i_{Ls}) is set by the real current zero-crossing at the time instant t_3, which leads to a state change from S6 to S5. During the time interval $t_3 < t < t_4$, C_U is discharged and C_D is charged. At the time instant t_4, the charging and the discharging are completed and D4 begins to be conductive. During the time interval $t_4 < t < t_6$, the resonant current flows via T1 and D4. At the time instant t_5, the transistor T4 turns on under ZVS condition and the converter state changes from S5 to S1. The start-up phase is completed.

3.4. Distorted Resonant Current and Multi-Zero-Crossings

The measured resonant current is usually distorted by its high order harmonic components and the noises introduced by the power- and measurement circuit, which results in multi-zero-crossings of the resonant current (Fig. 7a). This problem is solved by disabling the cur-

rent zero-crossing detection block for a time interval T_{lock} as soon as the first zero-crossing is detected (Fig. 7b and Fig. 7c).

4. Experiment Results

The novel full digital OM control unit is implemented under a dSPACE® rapid prototyping control system (RCP) including a processor board and a FPGA board. The processor board performs the standard voltage control task and outputs the duty cycle *D*. The proposed OM control strategy is implemented on the FPGA board, which reads the duty cycle value from the processor board and generates transistor gate signals. A SPRC prototype with a rated power of 32 kW is built for testing the novel full digital OM control unit.

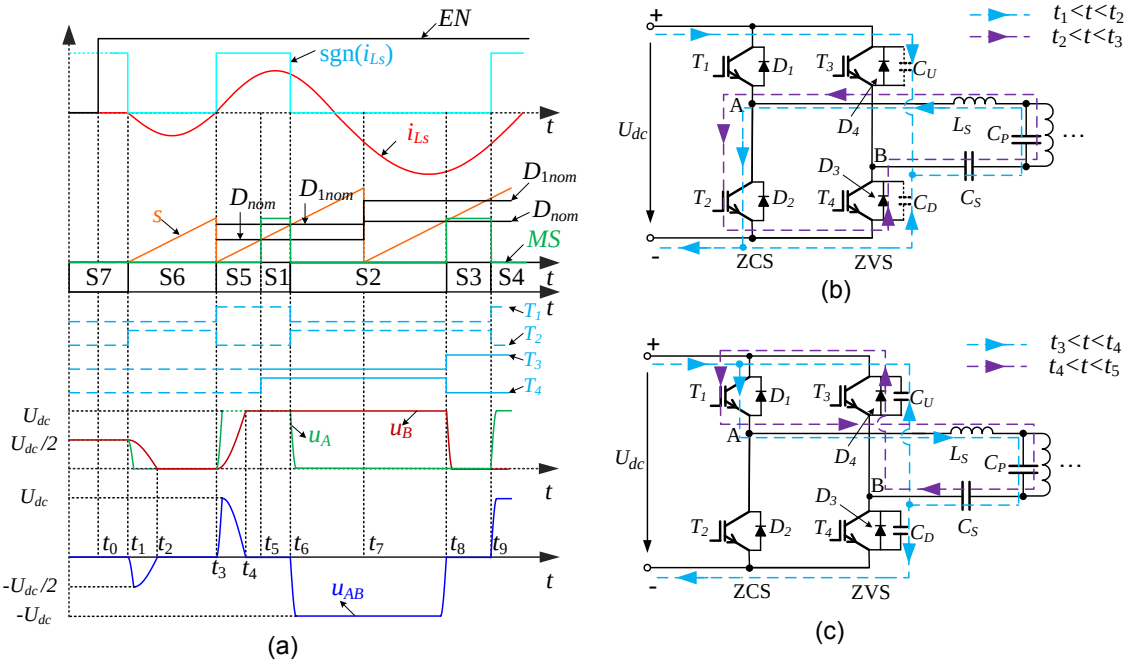


Fig. 6. Working principle and waveforms of the start-up operation mode

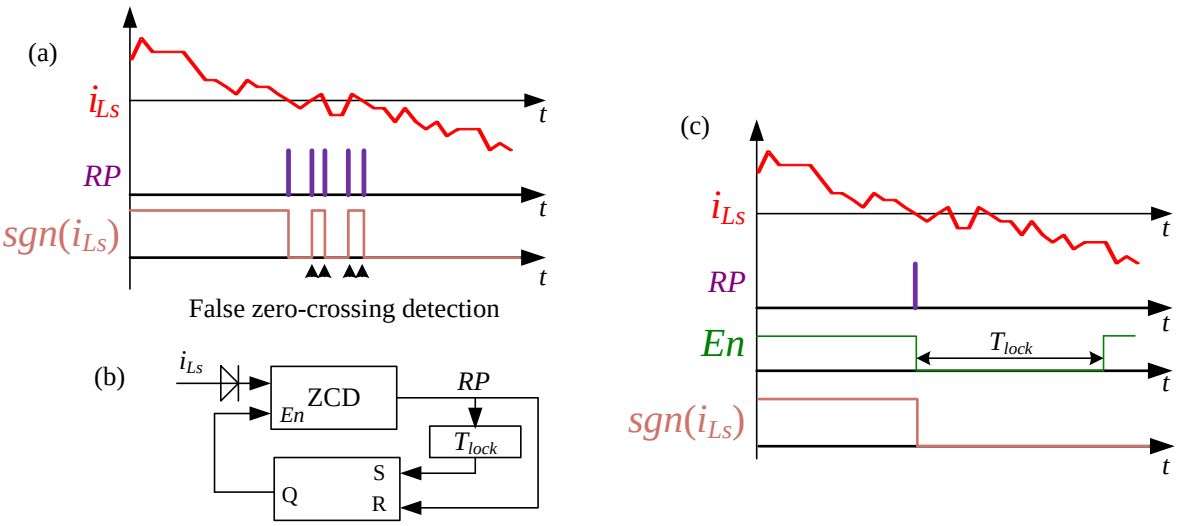
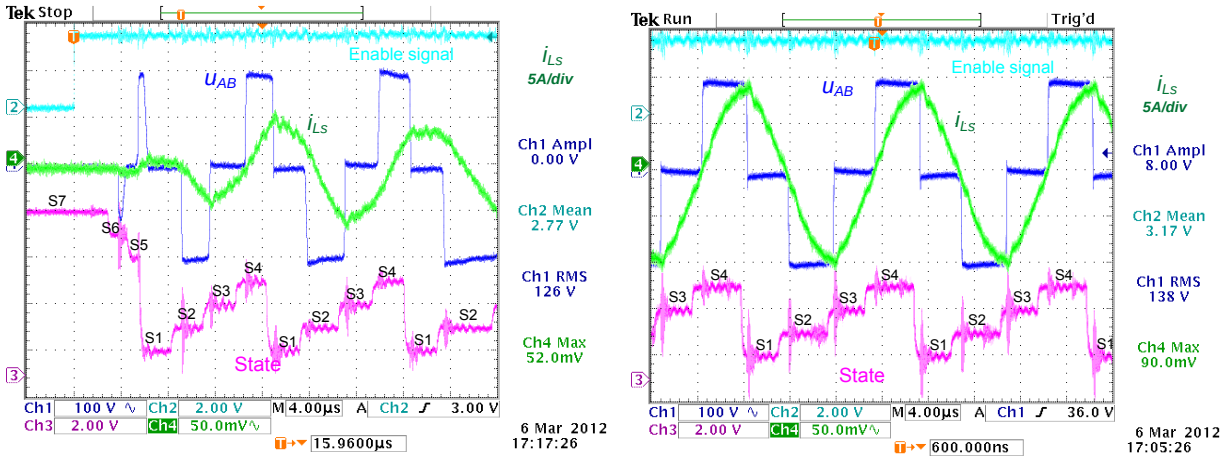


Fig. 7. (a) False and (b, c) revised current zero-crossing detection



(a) (b)

Fig. 8. Experimental results (a) in a start-up phase and (b) under steady-state operation

Oscillograms of the start-up phase and under steady-state operation are given in Fig. 8a and Fig. 8b, respectively. Resonant current i_{Ls} and inverter output voltage u_{AB} are directly measured in the power circuit. Enable signal and converter states are output from the FPGA board via a high-speed digital-analog converter (10 ns resolution). The measurement results show a good agreement with the theoretical analysis:

- State machine works well in the start-up phase and under steady-state conditions
- ZVS is ensured in the ZVS-leg in start-up phase
- ZVS and ZCS are achieved under steady-state operation

5. Conclusion and Future Works

In this contribution, a novel full digitally implemented OM control unit for SPRC is developed and implemented on a FPGA. Compared to the state-of-the-art hybrid solution, the novel full digital version has the following advantages:

- Increased system integration grade due to elimination of the analog circuit
- Increased design flexibility to implement additional functions, e.g. time delay compensation, correction of current zero-crossing detection errors, etc.
- Low distortion in the sawtooth signal and high response to resonant current frequency variation are achieved at the same time

In order to minimize turn-off losses of the ZVS-leg by utilizing capacitive snubbers, the state-of-the-art OM control strategy is extended with a special operation mode for the start-up phase. Using this extended OM control strategy, zero-voltage switching is ensured under all operation conditions for the ZVS-leg, incl. start-up, steady-state and transients, and zero-current switching is achieved for the ZCS-leg under steady-state operation. All functionalities of the novel full digital OM control unit are proved experimentally.

Acknowledgment

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under grant agreement number 232377. Particularly, the authors would like to thank C. Gmünder, R. Dörig (Regatron AG, Rorschach, Switzerland) and all other project partners for the intensive technical discussion and good cooperation.

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