ZVZCS Isolated Converter for Renewable Energy System with Extra Wide Voltage Range

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Abstract — A novel isolated current-fed full-bridge DC-DC converter with wide input voltage range for the applications of renewable energy system is proposed. The voltage transient spikes across the current-fed bridge and the current stress of the current-fed side switches are limited by auxiliary active clamping circuits on both sides, and ZVZCS is achieved. The operating principles and design considerations are discussed and verified by simulations and measurements.

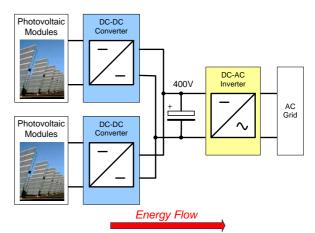
I Introduction

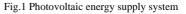
In applications such as solar arrays and fuel cells employed to feed energy to the AC grid, the 100Hz or 120Hz ripple in the output power of a single-phase inverter result to a large filter keeping the ripple in an acceptable range, which leads to noticeable efficiency restrictions. In order to minimize the voltage ripple and to compensate the variant output voltage of these energy sources, an isolating DC-DC converter controlled to yield a constant power flow is required to couple the energy source and DC-AC inverter in most cases.

In Fig. 1, a realization scheme for a solar energy system with two parallel stages is given. The DC-link (400V) is supplied by two converters operating in parallel. Each photovoltaic module with voltage range from 150V to 500V is controlled separately to operate on its own maximum power point (MPP) without synchronization. Certainly the PWM driving signal with one delayed phase of both (interleaved mode) can also be applied to minimize DC-link current ripple. The constant power flow is achieved by controlling DC-DC converter. On the AC side an

inverter is couples the generating system to the AC grid.

Compared to the voltage source DC-DC converter, the current source DC-DC convert can be applied in parallel operation without any special control mechanism used to guard correct power distribution, and the current ripple is also limited by the filter inductor. Considering these features, the isolated boost converter seems to represent a good circuit candidate for coupling the generating devices to the mains. Therefore high power current-fed full-bridge converters have become an important research topic during recent years [1] [6].





In order to design the current-fed isolated fullbridge converter, it is elementary to limit the high voltage transients across the bridge switches caused by switching actions in conjunction with the nonnegligible leakage inductance of the transformer due to the current feeding nature. This increases the switching stress and decreases the reliability. The simplest remedy is by employing a low leakage transformer together with RCD snubber to clamp the voltage, but a lower efficiency is the resulting drawback. A buck or a flyback converter is employed in industrial use for feeding the recovered energy of the clamping circuits back or forward to respective capacitors, but the resulting circuitry is rather complex [2] [3] [4].

In this contribution a current-fed full-bridge converter shown in Fig. 2 is proposed, improved by means of a simple auxiliary circuit including P_{aux} and two diodes at the voltage side, cooperating with an active clamp consisting of S_{aux} and C_{cl} on the current-fed side. By controlling the turn-off time of switches S1 and S3 the switches at the current-fed side are operated at ZVZCS. Moreover the resonant current between the clamping capacitor and leakage inductance is limited, thereby improving the converter efficiency significantly [5]. Between the current-fed full-bridge and input source a buck converter is employed for increasing the input voltage range.

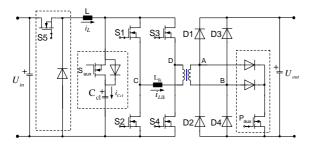


Fig. 2 Proposed current-fed full-bridge converter

II Principle of circuit operation

a. Boost mode operation

At the range of 150V to 400V, the converter is designed to work at boost mode, that means the filter inductor and full-bridge switches act as a current-fed converter, and switch S5 is turned on during this operation mode. Operation diagrams of the current-fed full-bridge are shown in Fig. 3, in which the buck converter is neglected. The phase shifted PWM serves as control means for the switches (S1~S4) of the current-fed full-bridge. The lower-leg switches S2 and S4 are operated at ZVS, and the upper-leg switches S1 and S3 are operated at ZCS, moreover the voltage stress of the switches are limited. The equivalent circuits and operation stages are shown in Fig. 4.

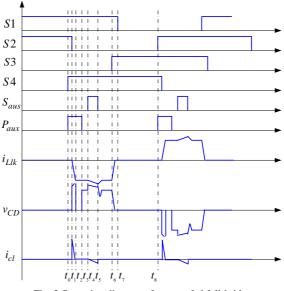


Fig. 3 Operation diagram of current-fed full-bridge.

Interval 0 [t < t₀]: Boost interval. Main switches S1and S2 are conducted, so boost inductor L is charged, and the transformer primary side is shorted. At t₀, S4 and P_{aux} is turned on, because the bridge is shorted also by S1 and S2, S4 is turned on at ZVS.

Interval 1 [$t_0 < t < t_1$]: After t_0 S4 and P_{aux} are on. But the boost inductor L is still charged.

Interval 2 [$t_1 < t < t_2$]: At t_1 , S2 is turned off. The parallel diode of switch S_{aux} conducts by freewheeling of boost current i_L , C_{cl} and L_{lk} resonate, then the current commutation begins.

Interval 3 [$t_2 < t < t_3$]: At t_2 , i_{Ccl} is zero and i_{Llk} equals i_L . In this interval, P_{aux} is still turned on, i_{Llk} is freewheeling.

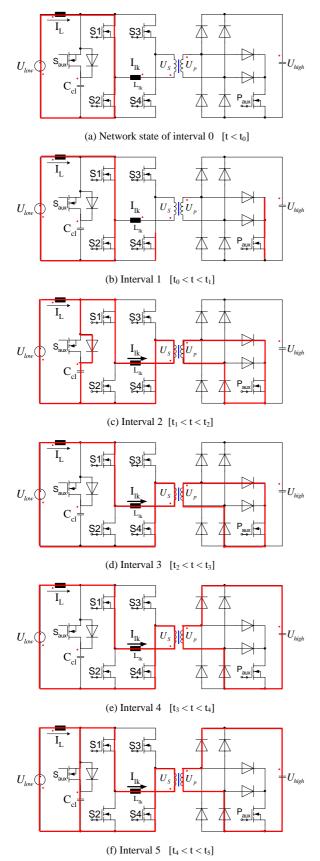
Interval 4 [$t_3 < t < t_4$]: At t_3 , P_{aux} is turned off. The energy is delivered to the DC-link.

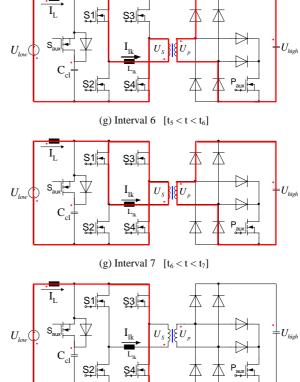
Interval 5 [$t_4 < t < t_5$]: At t_4 , S_{aux} is turned on, In this stage the clamping capacitor C_{cl} is discharged, the snubbed energy is then delivered to the DC-link.

Interval 6 [$t_5 < t < t_6$]: At t_5 , S_{aux} is off. The energy is still delivered to the DC-link. And in this mode, $i_{Llk} = i_L$.

Interval 7 [$t_6 < t < t_7$]: At t_6 , S3 is turned on by ZCS due to the leakage inductance. After S3 turned on, i_{Llk} is decreased to zero by the reflected voltage from the DC-link.

Interval 8 [$t_7 < t < t_8$]: After $i_{Llk} = 0$, S1 can be turned off by ZCS. The boost inductor L is charged. At t_8 , the next half period begins.





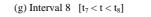


Fig. 4 Operation stages of boost mode.

b. Soft switching condition

The aforementioned ZVS of S2 and S4 occur in any load condition, because the current-fed bridge is shorted before S2 and S4 turn on.

In order to achieve ZCS of S1 and S3, The delay between the upper-leg current-fed switches should be longer than interval 7 [$t_6 < t < t_7$].

The minimum delay time is:

 $T_{d\min S1S3} = L_{lk} I_{L\max} / V_{CD} .$

d. Reduction of the snubbed energy

In interval 2 [$t_1 < t < t_2$] the high transient voltage occurs inevitably in Boost mode, which could be snubbed by the clamping branch (S_{aux} , C_{cl}). The snubbed energy of C_{cl} is transferred to the output via switches S1~S4, hence only a minor increase of current results for the switches. The auxiliary switch P_{aux} is employed to limit the snubbed energy, subsequently the current stress of primary side clamp can be reduced as well as the voltage stress on the full-bridge switches. This has a pronounced effect on η .

The transformer is clamped, when P_{aux} conducts. Hence voltage u_s equals zero, the leakage inductance current i_{Llk} increases sharply, and the clamping capacitor current decreases quickly. As the commutation interval reduced, the dynamic response and the efficiency of converter will be increased.

c. Clamping capacitor

During the rise time of i_{Llk} , the clamping capacitor is charged. In order to keep the voltage peak of fullbridge switches to desired range, the value of the clamping capacitor is selected as:

$$C_{cl} \approx \frac{L_{lk} * (I_{L_{\max}})^2}{U_{cl} * \Delta U_{cl}}$$

d. Extension of input voltage range

In the case that the input voltage is increased to $400V \sim 500V$, the converter is operated at extended voltage mode, by which requires a pre-connected buck converter. Operation diagrams of the current-fed full-bridge are shown in Fig. 5.

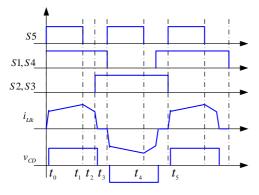
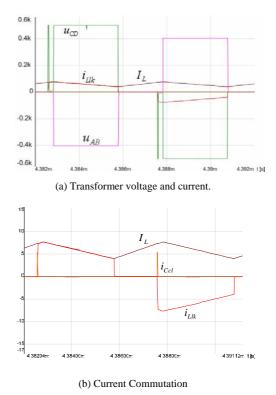
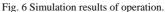


Fig. 5 Operation stages at extended voltage mode.

III Simulation

To verify the theoretical analysis of the proposed topology simulation models are built in SIMPLORER using the following design specification: $u_{in} = 300V$, $U_{out} = 400V$, $L_{lk} = 0.5\mu H$, $L = 170\mu H$, $C_{Cl} = 2\mu H$. Simulation results of the boost mode operation are shown in Fig 6, in which the transformer primary side voltage u_{AB} and secondary side voltage u_{CD} , leakage inductance current i_{Llk} , clamping capacitor current i_{Ccl} and voltage u_{Ccl} are displayed.





The simulation results show that the clamping circuits allow a major reduction of the voltage stress of main switches, moreover the current commutation between boost inductor and leakage inductance is accelerated. Hence, the converter could be operated with a high switching frequency up tp 100 kHz.

TABLE I

Component		Value
$S_1 \sim S_4$	COOL MOSFET	SPW35N60C3
P_{aux} , S_{aux}	COOL MOSFET	SPW20N60C3
C _{cl}	snubber capacitor	2µF
n	transformer turns ratio	1:1
L _{lk}	leakage inductance	0.5 <i>µ</i> H
f_s	Switching frequency	50 kHz

IV Experimental results

A 2.5kW experimental prototype was built to verify the operation principle of the proposed converter. A photovoltaic module working at the current-fed side is employed as energy supply element, whose voltage range is $150 \sim 500$ V. The DC-link voltage is controlled to be 400V. The parameters of circuit are listed in table 1.

The complete control scheme block diagram is shown in Fig. 7, which is integrated with the average current and voltage control of the PV module for MPP tracking. A two loop control scheme is used in order to control the energy flow and to improve the system dynamic behavior and stability.

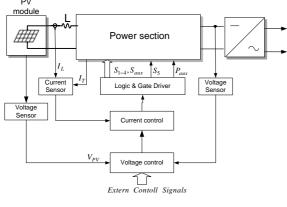


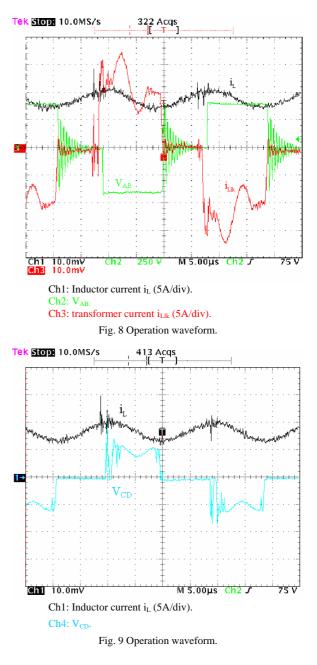
Fig. 7 Control scheme

The DC-bus voltage and the voltage of the energy storage element are sampled as voltage feedback. The current of inductor L is employed as current feedback. The current control loop of boost mode is implemented by using phase shift PWM IC UCC3895 which acts as current compensator and PWM modulator. The gate drive signals of the auxiliary switches shown in Fig. 3 are generated by a CPLD, which is employed also to monitor the fault signals of the converter and to perform the protection scheme.

In order to avoid the saturation of the transformer in case of an asymmetrical voltage-second product, a dynamic control of the magnetizing current of transformer is realized in conjunction with boost inductor current control. The effective duty-cycles of main switches are regulated by an additional slight variance of the control signal in case of an asymmetrical current sensed.

The experimental waveforms of the input inductor current, the current-fed side transformer current and transformer secondary side voltage are shown in Fig. 8, and the transformer primary side voltage and inductor current are shown in Fig. 9.

From the experiments, it can be seen that the voltage peaks caused by transformer leakage inductance are reduced by the clamping circuit, moreover the interval of the current commutation is reduced greatly. The waveform of transformer current is determined by the turn-on interval of clamping switch S_{aux} , which need to be optimized further.



V Conclusion

In this paper, a novel isolated full-bridge boost dcdc converter using phase shifted PWM control is presented. By using appropriate clamp circuits at current-fed and output side, the voltage transient spikes across the circuit-fed bridge are limited, and all switches are operated at soft switching. The operating principles and design considerations are discussed and verified by simulation and experiment.

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