Enhanced Analysis and Design Issues of a 3-Level DC/DC Converter with Zero Voltage and Zero Current Switching

N. Fröhleke

Institute of Power Electronics and Electrical Drives
University of Paderborn
Pohlweg 47-49
33098 Paderborn
froehleke@lea.upb.de
www.lea.upb.de

M. Schniedermann

Ascom Energy Systems
Coesterweg 45
59494 Soest
marc.schniedermann@ascom.de
www.ascom.com

Acknowledgement

The authors acknowledge gratefully the financial support granted by the European Commission under project BRST- CT98 5310, the co-operation with University of Leuven and the support by the industrial partners of the consortium.

Keywords

High frequency power converters, Multilevel converters, Switched-mode power supplies, ZCS converters, ZVS converters

Abstract

An enhanced analysis for a recently proposed, 3-level half bridge featuring reduced voltage stress and soft switching of the transistors is presented revealing additional network states and yielding more exact dc-voltage ratio. Practical design issues such as downsizing a bulky auxiliary capacitor and a flying capacitor is addressed after stress quantities are given. Experimental results gained on a 140A/4kW prototype for welding power supplies are presented.

I. Introduction

Due to the degrading of power line voltage quality resulting from the increasing currents drawn by power electronic loads standards were enforced on the maximum tolerable harmonic distortion. In order to comply with these standards the so called front-end AC/DC converters comprise nowadays PFC-switched mode rectifiers (SMR) to source 3-phase distributed power systems or simply medium power applications. Some topologies used in PFC-SMRs such as the 3-phase single switch boost rectifier require a larger boosting of the output voltage in respect to the input voltage for reduction of the harmonic distortion as compared to the 3-phase 3-level boost rectifier (also known as the Vienna rectifier), which means that operation on the European utility the dc-link voltage reaches 740 – 850 Volts.
Hence, the switching devices of the succeeding DC/DC-converter providing galvanic isolation and dc output voltage regulation - in case of welding power supplies current regulation - are charged by high voltage stress at high switching frequency. The latter arises of course by the objective to miniaturize the bulky hf-driven power transformer. And since the authors gained good results from the viewpoint of electrical performance as well as of economics for the front-end by using the 3-level switching approach, it is logical to apply a 3-level scheme to the DC/DC conversion stage, too. This because the available semiconductor devices switched at high frequency favor the use of 3-level schemes. But it still needs investigation of typical applications, whether the impact on volume shrinking for power transformer and output filter and costs is as pronounced as for the input filter for PFC-SMRs, where strict standards are to be fulfilled.

However, for high voltage dc rail input, typical for dc-dc-converters fed by power factor correctors, the three-level ZVS-ZCS-halfbridge converter depicted in Fig. 1 is a promising topological candidate due to low voltage stress on the switches and reduced switching losses. A well written overview about the literature on topologies for medium to high power range, supplemented by qualitative statements on pro and cons of the various circuits, a brief analysis as well as results obtained on a 6kW / 100kHz prototype were presented in [1] for e.g. topology. But neither formulae for calculating the peak currents in the primary sided components were given nor were problems addressed caused by the bulky auxiliary capacitor C_{aux}. This paper presents an analysis considering an auxiliary capacitor just big enough to assure operation under worst-case conditions.

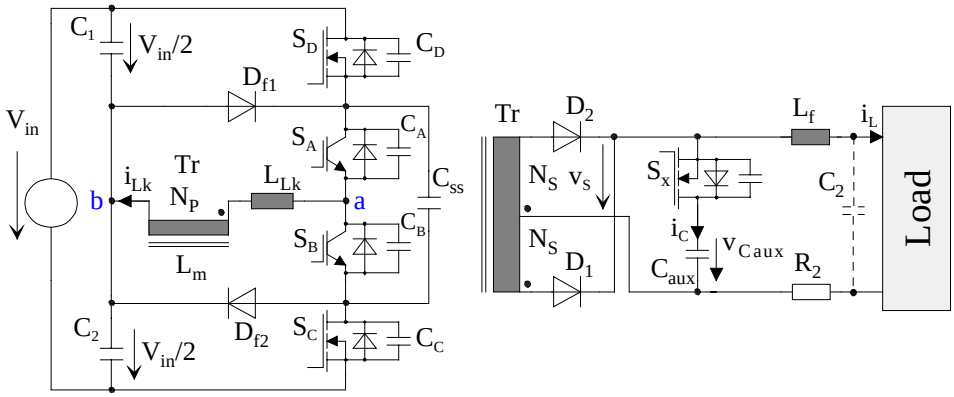

Fig. 1 Power circuitry of the 3-Level ZVS/ZCS-Halfbridge

II. Working principle

As shown in Fig. 1, the two inner switches, S_A and S_B, and the two outer switches, S_C and S_D, are operated exactly as if they were used in a phase shifted fullbridge [2]. Thus, without additional effort, zero voltage switching (ZVS) is achieved for S_C and S_D. Whenever a freewheeling interval is entered, however, the auxiliary switch S_x is activated for a short fraction of the conversion cycle in order to reset the undesired freewheeling current on the primary side of the transformer, achieving zero current switching (ZCS) for S_A and S_B. The flying capacitor C_{SS} assures that none of the switches is subjected to more than half the input voltage at any time. Note, that this holds only, if diodes D_{f1} and D_{f2} clamp C_{SS} at least once per conversion cycle to $V_{in}/2$, implying that the duty cycle must be limited.

III. Analysis

For steady state analysis of the converter all components are assumed to be ideal, if not otherwise stated.

- Since the ripple of the output filter current is small, the output filter is replaced by a constant current source I_L.
- The transformer turns ratio is $n = N_S / N_P$. An inductance L_{Lk} models the leakage inductance seen by the primary, while the magnetizing current is neglected.
- Capacitors C_1, C_2, and C_{SS} are large enough to be replaced by voltage sources $V_{in}/2$. Output capacitances of the switches, however, are considered.

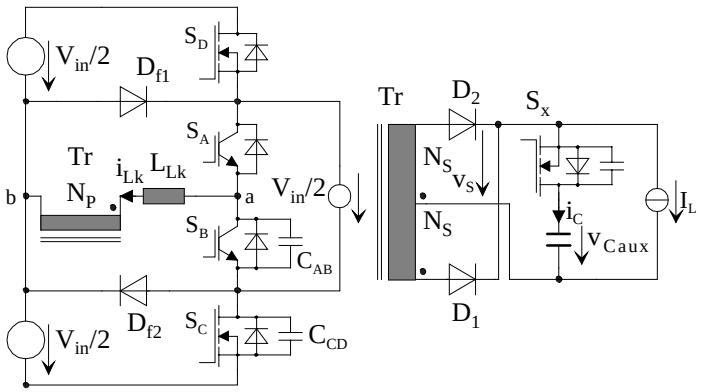

Fig. 2 Power circuitry using simplifying assumptions

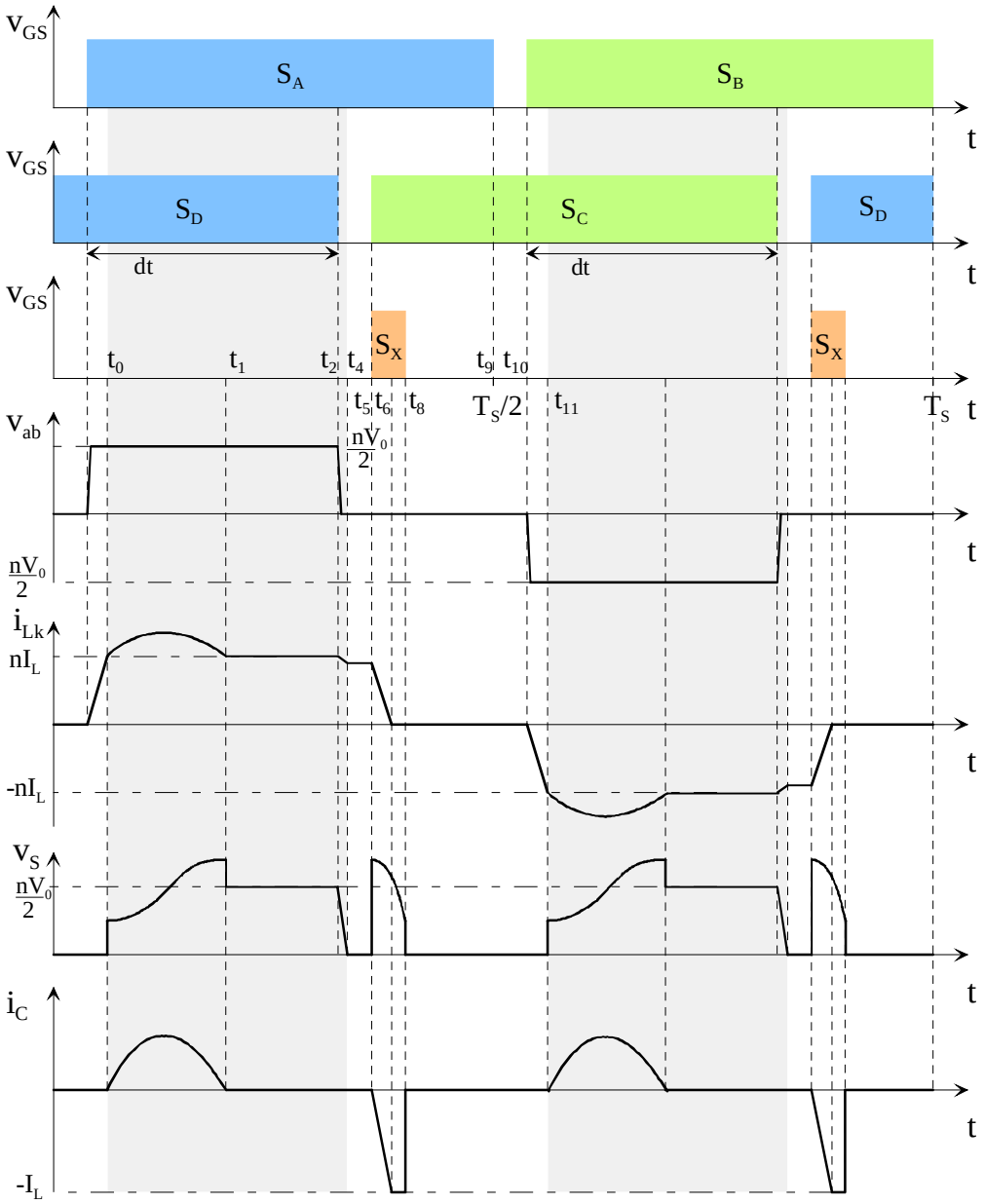

Fig. 3 Gating signals and principle waveforms

Since reducing the size of auxiliary capacitor C_{aux} is a main target of this paper, a substantial voltage ripple is allowed across C_{aux}. Fig. 2 shows the simplified power circuit, with $C_{AB} = C_A + C_B$ and $C_{CD} = C_C + C_D$ as a consequence of constant voltages across C_1 and C_2, further simplifying the analysis without loss of accuracy. But since the equivalent circuits do not reflect the physical identity any longer comments are given concerning to the charging/discharging of resp. transistor capacitances.

With the chosen gating scheme, the conversion cycle divides into 11 states, depicted in Fig. 2. In order to keep the analysis within manageable limits, the analysis here focuses on most important intervals.

Interval 1 [t_0, t_1]: Power transfer and charging of C_{aux}

At t_0, switches S_A and S_D are conducting and primary current i_{Lk} equals the reflected load current $n \cdot I_L$, yielding equivalent circuit depicted in Fig. 4. Since the voltage ripple across capacitor C_{aux} is substantial, at t_0 body diode D_x of auxiliary switch S_x starts to conduct, giving rise to resonance between leakage inductance L_{Lk} and auxiliary capacitor C_{aux} yielding

$$i_{Lk}(t) = n \cdot I_L + I_{Pk} \cdot \sin(\omega_0 \cdot t) \qquad \text{(Eq. 1)}$$

with angular frequency $\omega_0 = 1/\sqrt{L_{Lk} \cdot n^2 C_{aux}}$ and peak resonant current I_{Pk}, which is determined in section “Design consideration”.
After one half cycle, at $t_1 = \pi/\omega_0$ resonance terminates by blocking of D_x. During resonance, C_{aux} is charged from v_{Caux0} to v_{Caux01}.

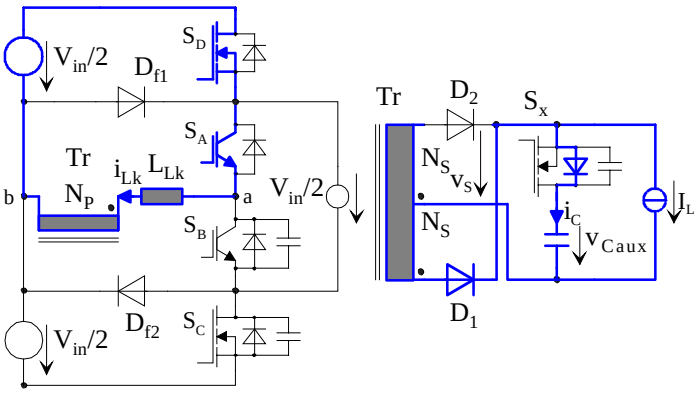

Fig. 4: Equivalent circuit in interval 1

Interval 2 [t_1, t_2]: Power transfer

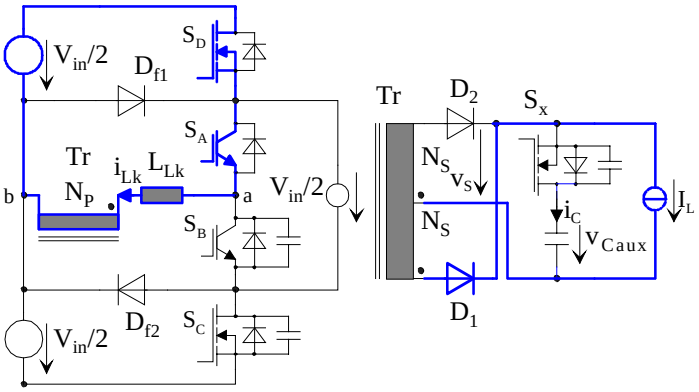

Fig. 5 Equivalent circuit in interval 2

During this interval, the auxiliary circuit is passive, as depicted in Fig. 5. Since magnetizing current is neglected, $i_{Lk} = n \cdot I_L = const.$ throughout the interval, until at t_2 the interval is terminated by the modulator, depending on the phase shift. The antiparallel diode of S_x blocks voltage $v_{C\,aux}$.

Intervals 3 [t_2, t_3] and 4 [t_3, t_4]: Charging, discharging of transistor capacitances

At t_2 the modulator opens switch S_D, yielding equivalent circuit depicted in Fig. 6. Capacitor C_{CD} is discharged, thus ZVS for S_C, and in the second half conversion cycle for S_D, is assured.

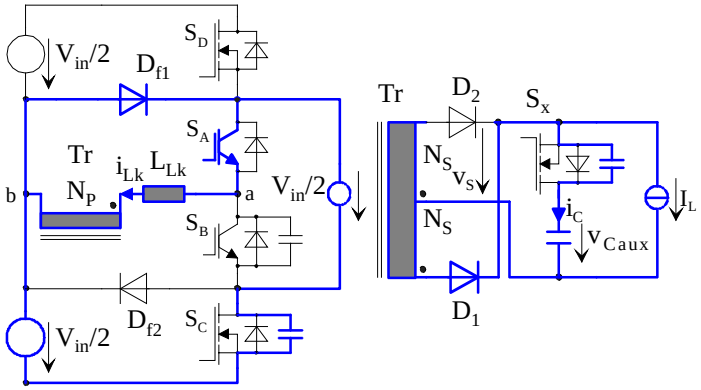

Fig. 6 Equivalent circuit in interval 3

Along with transformer primary voltage v_{ab} rectifier voltage v_S approaches zero. At t_3 commutation on the primary side of the transformer is completed and D_{f1} conducts; switch S_C is switched on under zero voltage conditions with it´s body diode becoming conductive. The output capacitance C_X of transistor S_X, however, is still charged until t_4, causing a small decrease in primary current i_{Lk}.

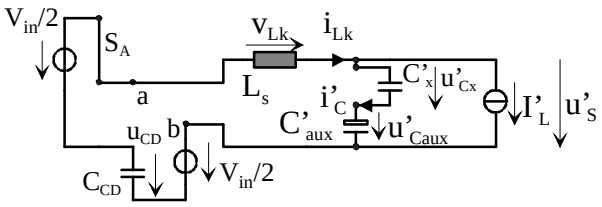

Fig. 7 Equivalent circuit for intervals 3 and 4 (further simplified)

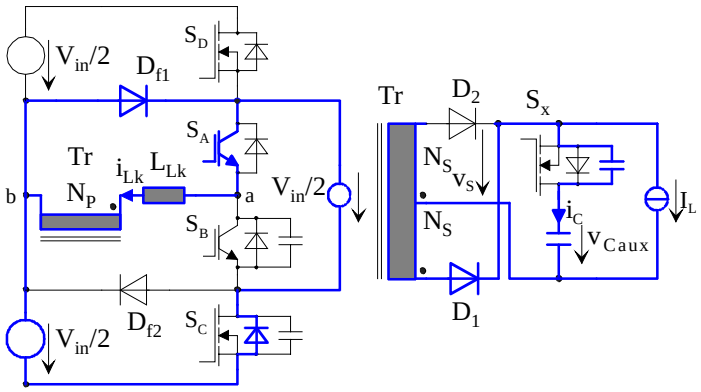

Fig. 8 Equivalent circuit in interval 4

Fig. 7 shows an equivalent circuit to demonstrate the concurrent resonances between C_{CD}, C'_X and L_{Lk}, with $C'_X = n^2 \cdot C_X$. Note, that C_{CD} is charged almost linearly since i_{Lk} is practically constant

during these intervals, while C'_X resonates with L_{Lk}. With practical part values, C_{CD} will be discharged before C'_X, yielding equivalent circuit depicted in Fig. 8.

Intervals 5 [t_4, t_5] and 6 [t_5, t_6]: Freewheeling, ZVS of S_C and commutation

At this reduced current level, both primary and secondary side enter freewheeling modes, which are terminated at t_5 by switching on the auxiliary transistor S_X. Applying v_{Caux01} to the rectifier initiates resonance between leakage inductance L_{Lk} and capacitor C_{aux} very similar to the resonance in [t_0, t_1].

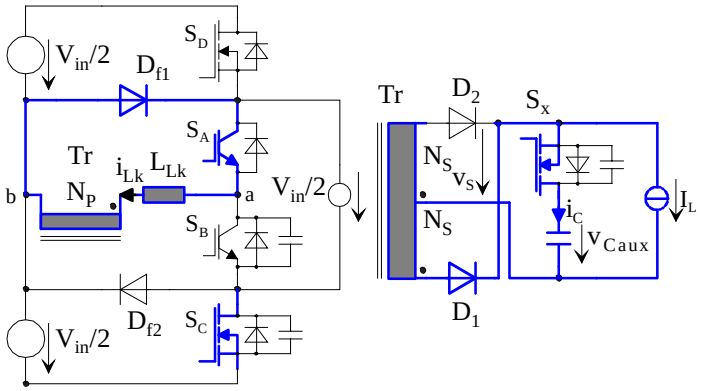

Fig. 9 Equivalent circuit in interval 5 and 6

Since $v_{C\,aux}$ is applied to L_{Lk}, primary current i_{Lk} is reduced to zero at t_5, thus terminating freewheeling on the primary rapidly. In principle, S_X could be switched off at t_6, but since fast detection of zero current is difficult, a constant conduction time T_{OnSx} was implemented for S_X. Therefore, from t_5 to t_6, with $t_6 - t_4 = T_{OnSx}$, capacitor C_{aux} delivers the total output current, further discharging C_{aux}.

Intervals 7 to 11 [t_6, t_{11}]:

When switching off S_X at t_7, the output current I_L commutates back to the rectifier diodes, which start freewheeling. Since primary current i_{Lk} had been eliminated, at t_9 transistor S_A is switched off under zero current conditions. Finally, at t_{10} the modulator activates S_B, which is also operated under zero current conditions. Primary current i_{Lk} rises linearly up to the reflected output current $n \cdot I_L$ at t_{11}, starting a new conversion half cycle. Due to the minor influence of this network states on the output voltage and current they are omitted here (refer to [1])

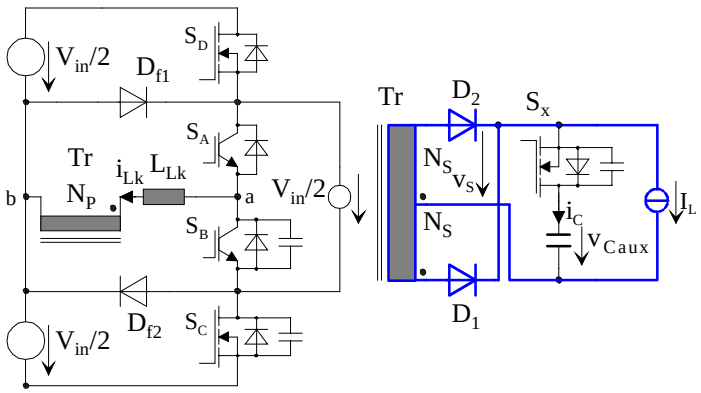

Fig. 10 Equivalent circuit in interval 7 and 11

IV. Modeling and control

For modeling the method of effective duty cycle was used, with effective duty cycle being computing by summarizing the duration T_i of the separate intervals i over half a conversion cycle yielding $D_{eff} = \frac{2}{T_S}\sum_{i=0}^{11} k_{vs,i} T_i$. However, the modeling effort showed to have minor importance, since both simulation and measurement results indicate a dominant influence at least in case of R/L nature of the load for a welding power supply. For various reasons, including stability and immunity to noise, an average current mode control scheme was used parameterized according to [5]. Controller parameters $K_R = 28700$, $\omega_Z = 5410 \cdot s^{-1}$, and $\omega_Z = 105000 \cdot s^{-1}$ yielded excellent dynamic response, naturally limited, however, by output voltage swing and load parameters.

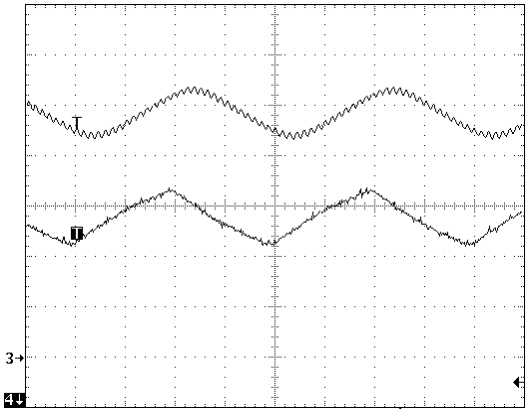

Fig. 11 Closed loop performance: Ch3 (below)= set point, Ch4 (above)=Load current (10A/Div)

V. Design considerations

An important design issue is the downscaling and proper selection of the auxiliary capacitor C_{aux}. As the resonance between C_{aux} and leakage inductance L_{Lk} can lead to considerable current stress for primary switches, rectifying diodes, and body diode of auxiliary switch S_X.

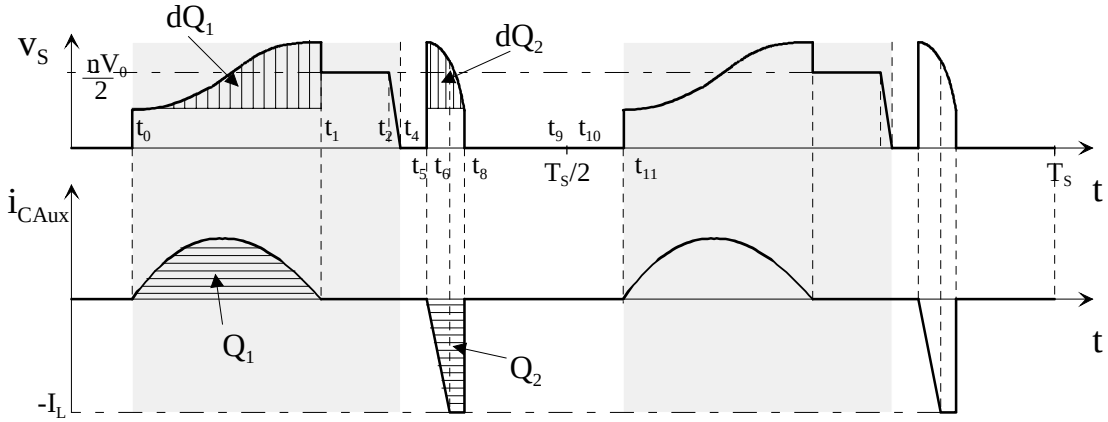

Fig. 12 Waveforms to calculate the current peak

According to Fig. 12, the peak current I_{Pk} is determined by using steady state condition for $v_{C\,aux}$ with

$$\int_{t=0}^{t=\pi/\omega_0} i_{Pk} \cdot \sin(\omega_0 \cdot t)dt \equiv n \cdot I_L \cdot (T_{OnSx} - \frac{t_{demagn}}{2}), \qquad \text{(Eq. 2)}$$

when assuming a linear decrease of freewheeling current i_{Lk} during demagnetizing time t_{demagn}, yielding $i_{LkPeak} = \frac{\omega_0 \cdot n \cdot I_L}{2} \cdot (T_{OnSx} - \frac{t_{demagn}}{2})$. Thus, the additional current peak caused depends only on conduction time of S_X and load current I_L, as well as on losses in real live.

VI. Verification

A laboratory prototype was built to be applied as welding power supply with maximum output current of 140A at 4kW output power fed from 3-phase mains at nominal 540V dc rail voltage, see block diagram depicted in Fig. 9.

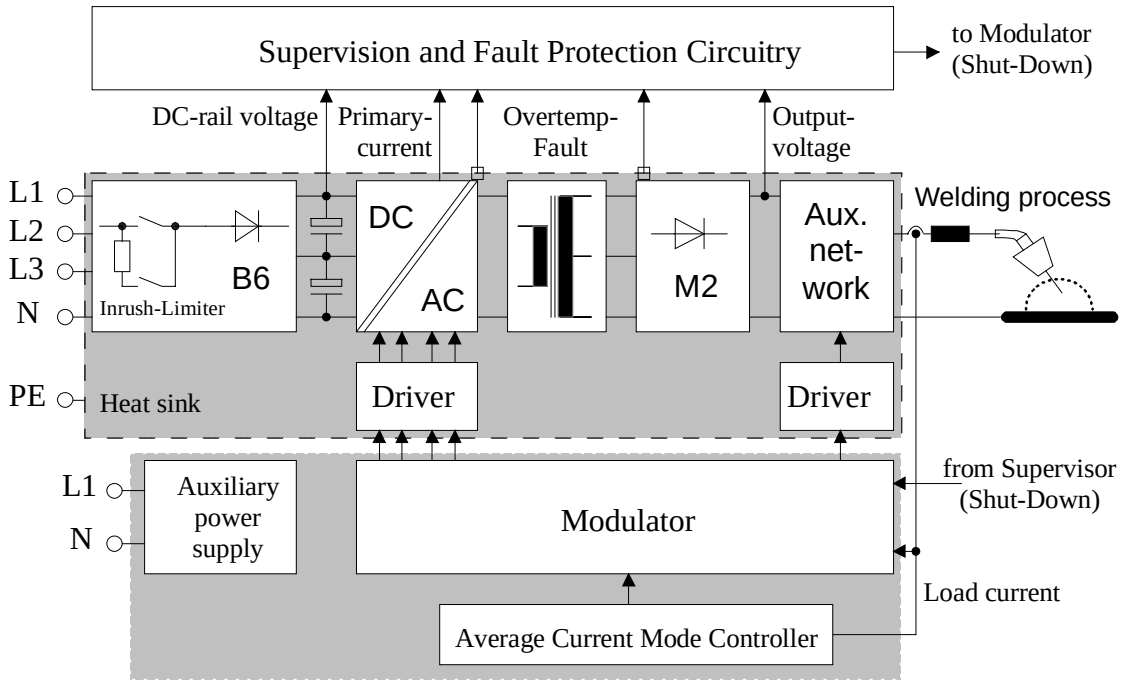

Fig. 13 Block diagram of the 140A/4KW prototype

Parts are as follows: $C_{aux} = 5 \cdot 0.47\mu F\ FKP$: $C_1 = C_2 = 2 \cdot 3.3\mu F$, $C_{SS} = 3.3\mu F$, Tr: PAYTON Magnetics Planar Transformer T1000 (1:7:7), S_X: IXFN100N25, $S_C = S_D$: STE38NB50, $S_A = S_B$: IXGN50N60B, $D_{f1,2}$: DSEI2x30-06C, $D_{1,2}$: DSS2x101-015A. While the primary current is sensed by a 1:200 current transformer for protection purposes, a LEM current sensor measures the output current. An Unitrode UC3985 phase-shift controller is employed with adaptable delay times, using average current mode control. Not realized due to technical problems, but nevertheless desirable, is adaptive control of the activation time for auxiliary switch S_X. In order to minimize current stress for a number of components, T_{OnSx} should be chosen just big enough to ensure demagnetization of L_{Lk}. Since i_{Lk} is approximately $n \cdot I_L$ prior to demagnetization, and also v_{Caux} and L_{Lk} are roughly known, load current I_L may be used to control T_{OnSx} appropriately. This, however, is only viable if the value of the passive components are chosen carefully.

During building of the prototype careful circuit layout proved to be vital for circuit behavior. In particular, additional stray inductance on the secondary side of the transformer had a tremendous influence on the effective stray inductance simply by being multiplied by $1/n^2$. In turn, the angular frequency ω_0 was much lower than expected. Nevertheless, if the correct value of L_{Lk} is used the results of analysis, simulations (by SIMPLORER, see Fig. 11) and measurements (obtained on the prototype, see Fig. 12) match very well.

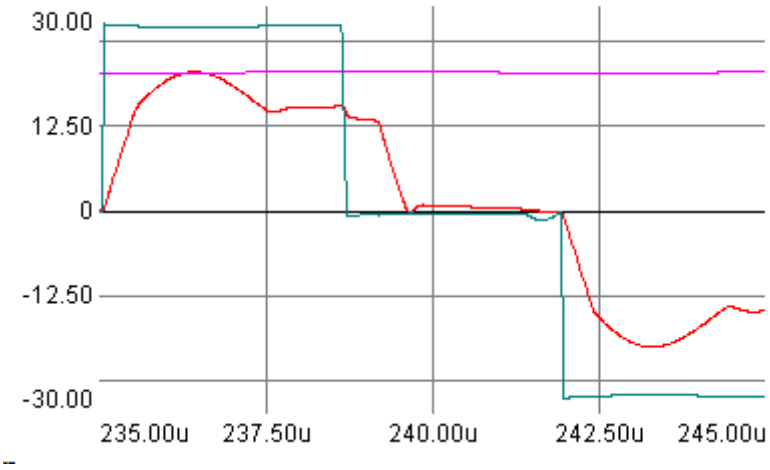

Fig. 14 Simulated waveforms: i_{Lk} (red in A); v_{ab}/10 (grey in V); I_L/5 (pink in A)

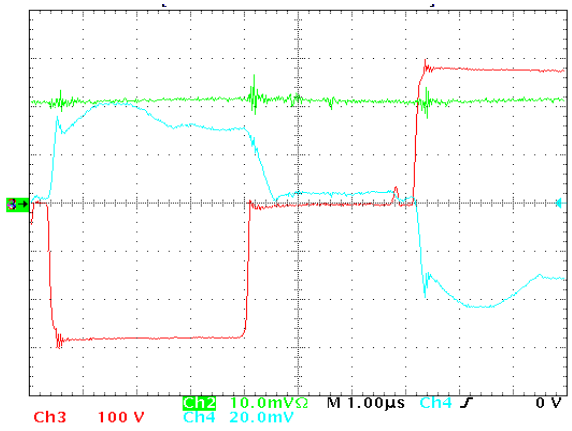

Fig. 15 Measured waveforms: Ch2: I_L (50A/Div); Ch3: $-v_{ab}$ (100V/Div); Ch4: i_{Lk} (10A/Div)

Note, that the difference between simulated waveforms and measurements in Fig. 14 and 15 are not large when applying an IGBT with an antiparallel connected fast diode, while a large reverse recovery of the inherent diode turned up, when a power MOSFET is used as auxiliary switch. The total breadboard assembly is shown in Fig. 16.

Summary and Outlook

The presented enhanced analysis forms a base in finding a compromise between the size of the auxiliary capacitor for commutation and the resulting higher current stress for the power rail for optimizing the recently introduced ZVSCS 3-level DC/DC converter. It presents a good counterpart topology to 3-phase medium to high power switched mode rectifiers as IGBTs can be utilized at high switching frequency. By using improved driver circuits and control logic the gained efficiencies should be boosted.

Fig. 16 Prototype of a 140A/4kW Welding Power Supply (left: input filter and rectifier, right: DC-DC Converter

References

[1]. F. Canales, P. M. Barbosa, F.C. Lee: „A Zero Voltage and Zero Current Switching Three Level DC/DC Converter“, Conf. On Applied Power Electronics, APEC, 2000, pp. 314-320.

[2]. Unitrode / Texas Instruments: BiCMOS advanced phase shift PWM controller UCC18/28/3895, SLUS157 August 1999 (www.unitrode.com).

[3]. J.-G. Cho, C.-Y. Jeong, F. C. Y. Lee: „Zero-Voltage and Zero-Current-Switching Full-Bridge PWM Converter Using Secondary Active Clamp“, IEEE Trans. On Power Electronics, Vol. 13, No. 4, July 1998, pp. 601-607.

[4]. N. Fröhleke, H. Mundinger, a. o.: ”Resonant Transition Switching Welding Power Supply”, Int. Conf. On Industr. Electronics, Control, and Instrumentation, IECON, 1997, pp. 615-620.

[5]. Sun, J.,; Wu, W.-C.; Bass, R. M.: “Large-Signal Characterization of Single-Phase PFC Circuits with Different Types of Current Control”, IEEE Appl. Pow. Electr. Conf. and Exposition, 1998, pp. 655-660.