Pulse Width Modulation for Three-Phase Three-Level Converters

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ABSTRACT: Vector modulation is the most frequently used modulation scheme for three-level converters. If three-level converters are considered phase voltage modulation is advantageous because of its clear stepwise procedure in combination with an excellent insight into the internal processes of the converter. The computational demand is not more than with vector modulation

1 Introduction

In case of digital signal processing the reference voltages for PWM converters are normally delivered by the control as space vector components and accordingly vector modulation is applied to generate the switching signals for the power section. This is also true for three-level converters the basic circuit of which is shown in Fig. 1.

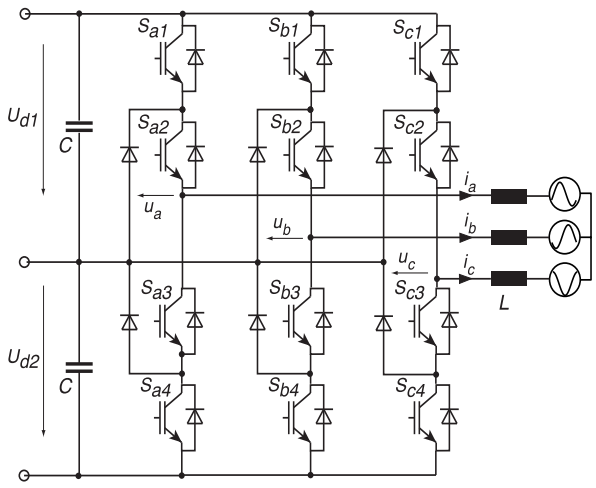

Fig. 1 Basic circuit of three-level PWM converter

Three level converters - inverters or rectifiers - are becoming more and more interesting because the blocking voltage of all transistors is clamped to half the dc-link voltage. This makes possible either to increase the dc link voltage or to improve efficiency by use of low voltage transistors having lower conduction and switching losses.
In the three level converter of Fig. 1 each phase voltage can be set to one of the three voltage levels of the dc link by switching on of a pair of transistors. This can be described by the simple equivalent circuit of Fig. 2, where the electronic switches are replaced by mechanical switches having three positions +, 0, -.

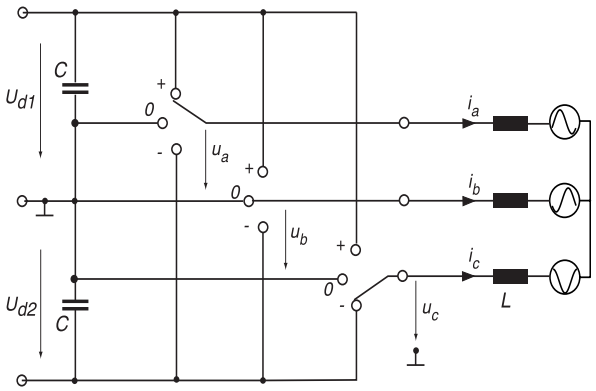

Fig. 2 Equivalent circuit of three-level converter

A survey on the achievable values of phase voltage and the related states of electronic switches of Fig. 1 and mechanical switches of Fig. 2 is given in Table 1

Table 1 Voltage levels and switching states of phase *a*

phase voltage u_a	active transistors	position of switch Sa
U_{d1}	Sa1, Sa2	+
0	Sa2, Sa3	0
$-U_{d1}$	Sa3, Sa4	-

Due to three phases each having three switching states the converter has $3^3 = 27$ switching states. In contrast with this large number of switching states not more than 19 different positions of the voltage vector can be achieved. These vectors are shown in and marked with the switching states of the three phases in Fig. 3.
Space vector representation of the output voltage is very suitable for modulation task but a clearer insight into the internal processes of the converter is achieved by consi-

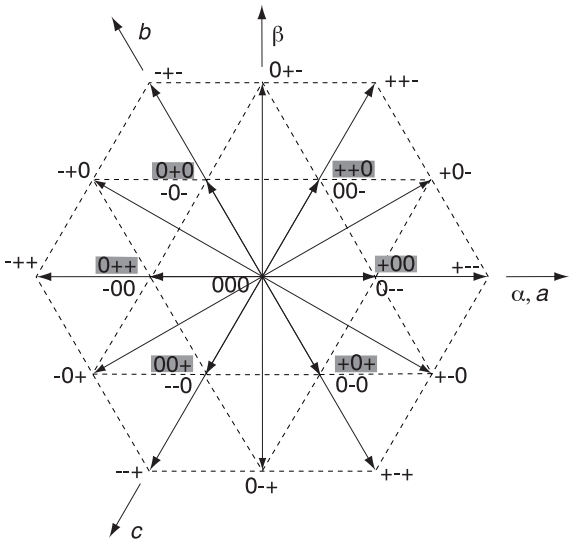

Fig. 3 Possible positions of voltage vector

dering the phase voltages. With regard to this aspect phase voltage modulation is investigated in this paper.

2 Normalization of phase voltages and generalization duty cycles

The required average output voltage $\overline{u}_a$ of phase a is generated by chopping mechanical switch Sa between positions '0' and '+' if $\overline{u}_a \geq 0$ is required. Positions '0' and '-' are used if $\overline{u}_a \leq 0$ is wanted (Note: $\overline{x}$ indicates local average values which result calculated for one switching period). In any case the characteristic of the converter is described in general by

$$\overline{u}_a = d_{a+} \cdot U_{d1} + d_{a-} \cdot U_{d2} + d_{a0} \cdot 0 \tag{1}$$

where d_{a+}, d_{a-}, d_{a0} are the duty cycles for switch positions '+', '-', '0', respectively.
Assuming symmetrical DC link voltages $U_{d1} = U_{d2} = U_d/2$ eq. (1) becomes

$$\overline{u}_a = (d_{a+} - d_{a-}) \cdot U_d/2 = d_a \cdot U_d/2 \tag{2}$$

where either d_{a+} or d_{a-} is zero. Keep in mind that d_a is a generalized duty cycle which can vary in the range $-1 \leq d_a \leq 1$.
From eq. (2) describing the behaviour of the power section we can derive the modulation algorithm

$$d_a = \frac{\overline{u}_a^*}{U_d/2} \tag{3}$$

which is used to derive the duty cycle from the reference of the average phase voltage $\overline{u}_a^*$ (Note: All references are marked by *).
According to eq. (2) duty cycle d_a is identical with the normalized average phase voltage $\overline{\mu}_a = 2\overline{u}_a/U_d$ which can vary in the same range as d_a, $-1 \leq \overline{\mu}_a \leq 1$.

3 Steps of phase voltage modulation

The algorithm of phase voltage modulation has to be established in such a way that the output voltages $\overline{u}_a$ $\overline{u}_b$, $\overline{u}_c$ equal the phase voltage references $\overline{u}_a^*$, $\overline{u}_b^*$, $\overline{u}_c^*$ which are delivered directly by the controller or which must be calculated from the components $\overline{u}_\alpha^*$, $\overline{u}_\beta^*$ of the reference voltage vector.
Phase voltage modulation is performed stepwise.
At the first step provisional values of generalized duty cycles d_a', d_b', d_c', i.e. normalized phase voltages $\overline{\mu}_a'$, $\overline{\mu}_b'$, $\overline{\mu}_c'$, are determined from the reference of voltage vector components.

$$\begin{bmatrix} d_a' \\ d_b' \\ d_c' \end{bmatrix} = \begin{bmatrix} \overline{\mu}_a' \\ \overline{\mu}_b' \\ \overline{\mu}_c' \end{bmatrix} \qquad \begin{bmatrix} \overline{\mu}_a' \\ \overline{\mu}_b' \\ \overline{\mu}_c' \end{bmatrix} = \frac{2}{U_d} \cdot \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} \overline{u}_\alpha^* \\ \overline{u}_\beta^* \end{bmatrix} \tag{4}$$

These values are provisional and may be out of the realizable range $-1 \leq d_a', d_b', d_c' \leq 1$. Furthermore, in particular when calculated from vector components, they do not include a zero component. This degree of freedom can be applied to shift the phase voltages without influencing the line voltages being applied to the load. In particular it can be used to shift the duty cycles into the permitted range.
To check the feasibility of phase voltages and duty cycles they are assorted now with respect to their values by determining the largest and the smallest voltage called $\overline{\mu}_x' = d_x'$ and $\overline{\mu}_z' = d_z'$, respectively.

$$\begin{aligned} \overline{\mu}_x' &= \mathrm{Max}\{\overline{\mu}_a', \overline{\mu}_b', \overline{\mu}_c'\} & \overline{\mu}_z' &= \mathrm{Min}\{\overline{\mu}_a', \overline{\mu}_b', \overline{\mu}_c'\} \\ d_x' &= \mathrm{Max}\{d_a', d_b', d_c'\} & d_z' &= \mathrm{Min}\{d_a', d_b', d_c'\} \end{aligned} \tag{5}$$

Thus we have established $d_x' \geq d_y' \geq d_z'$ i.e. $\overline{\mu}_x' \geq \overline{\mu}_y' \geq \overline{\mu}_z'$.
A typical switching pattern of normalized phase voltage having no zero component is shown in Fig. 4, where $d_x = -(d_y + d_z)$. Note that $d_x' \geq 0$ and $d_z' \leq 0$ is always true when no zero component is present and only $d_y' \leq 0$ is chosen abritrarily for this plot.

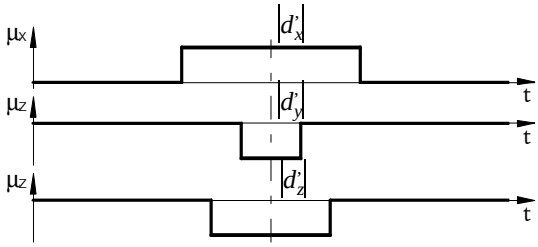

Fig. 4 Symmetrical pulse pattern without zero component

To achieve optimum usage of the operation range the normalized voltages are symmetrized now to $d_x'' = -d_z''$ by adding a zero component $d_0' = -(d_x' + d_z')/2$. This results in

$$d_x'' = \frac{d_x' - d_z'}{2} \qquad d_y'' = d_y' - \frac{d_x' + d_z'}{2} \qquad d_z'' = -\frac{d_x' - d_z'}{2} \tag{6}$$

Related shapes of phase voltages are shown in Fig. 5 where switching in phases x and z occurs exactly at the same instants. Note that $d_z = -d_x$ always holds and that the block of μ_y can be positive or negative, but is always smaller than the blocks of μ_z and μ_x.

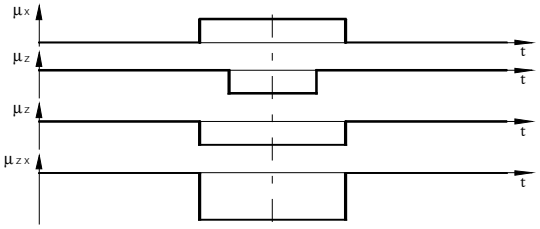

Fig. 5 Provisional symmetrical pulse pattern

Considering Fig. 5 feasability can be checked now easily:

- If $d_x'' = \overline{\mu}_x'' = 1$ is true, the maximum voltage level is applied because the smallest voltage is exactly at the lower limit, $d_z'' = \overline{\mu}_z'' = -1$.
- If $d_x'' > 1$ holds $\overline{\mu}_x''$ as well as $\overline{\mu}_z''$ are out of range. In this case all voltages can be reduced proportionally and we get the final values of generalized duty cycles i.e. normalized phase voltages

$$d_x = 1 \qquad d_y = \frac{d_y''}{d_x''} \qquad d_z = -1 \ . \tag{7}$$

- If $d_x'' < 1$ all duty cycles and voltages are inside the permitted range. In this case the voltage pulses can be shifted by adding or modifying a zero component $d_0 = \overline{\mu}_0$ until either $d_x = \overline{\mu}_x$ or $d_z = \overline{\mu}_z$ reaches the upper or lower limit, respectively.

$$d_x = d_x'' + d_0 \qquad d_y = d_y'' + d_0 \qquad d_z = d_z'' + d_0 \tag{8}$$

  Zero component d_0 is a degree of freedom which can be utilized to realize different goals which will be discussed in the section 4.
- When the final duty cycles are established, attention is drawn to the line voltages which are applied to the load and in particular the wave form of largest line voltage $\mu_{zx} = \mu_z - \mu_x$ generated by the largest and the smallest phase voltage is of interest.

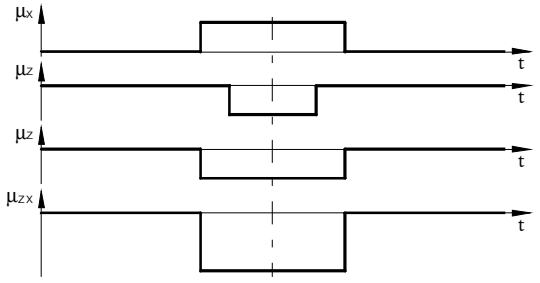

Fig. 6 Pulse pattern of Fig. 5 and related line voltage

In Fig. 6 the instantaneous phase voltages already shown in Fig. 5 are depicted again and the line voltage of interest is also given. From the plot it is obvious, that a large amplitude and large steps occur at line voltage μ_{zx} which is due to simultaneous switching at the involved phases z and x.

The large amplitude of μ_{zx} can be avoided when the negative blocks of voltage μ_z are shifted for half a switching period, see Fig. 7. Of course same phase shift

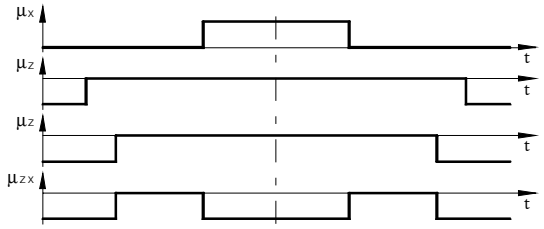

Fig. 7 Final symmetrical pulse pattern for low THD

is introduced for voltage wave of phase y because μ_y is also negative at this example.

After this phase shifting the phase voltages approach each other everywhere as good as possible causing the line voltages μ_{yz} and μ_{zx} to have more but lower steps. By this measure the THD is reduced and the ripple frequency is increased causing an additional reduction of current ripple without any influence on the local averages of the line voltages.

- At the last step the generalized duty cycles are reassessed from x, y, z to phases a, b, c according to the result of eq. (5) and are used to determine the duty cycles for the phase switches.

  This very last procedure is performed according to eq. (2). For phase a this equation is

$$d_{a+} - d_{a-} = d_a \tag{9}$$

which is evaluated in more detail in Table 2.

Table 2 Duty cycles for switches of phase a

d_a	d_{a-}	d_{a+}
$-1 \le d_a \le 0$	$d_{a-} = -d_a$	$d_{a+} = 0$
$0 \le d_a \le 1$	$d_{a-} = 0$	$d_{a+} = d_a$
Note: d_{a+} is the duty cycle for the upper switch of phase a which is not activated when $d_{a+} = 0$		

4 Choice of zero component

As already mentioned there are different goals which can determine the choice of zero component of the phase voltages.

- The harmonic content of the output voltage can be minimized by use of a symmetrical pulse pattern.
- The switching frequency and losses can be minimized if either $\overline{\mu}_x=1$ or $\overline{\mu}_y=0$ or $\overline{\mu}_z=-1$ is realized because now in phase x or y or z, respectively, no switching occurs.
- A special problem can be solved which has to be considered with three level converters: The center tap of the dc link is loaded by the current

$$\begin{aligned}\overline{i_0} &= (1-|d_a|)\cdot\overline{i_a}+(1-|d_b|)\cdot\overline{i_b}+(1-|d_c|)\cdot\overline{i_c} \\ &= -|d_a|\cdot\overline{i_a}-|d_b|\cdot\overline{i_b}-|d_c|\cdot\overline{i_c}\end{aligned} \tag{10}$$

  which causes the capacitor voltages to shift. During a switching period having the length T_S the change of capacitor voltages is given by

$$\Delta U_{d1}=-\Delta U_{d2}=\frac{\overline{i_0}\cdot T_S}{2C_d} \tag{11}$$

  To avoid unsymmetrical dc voltages either $\overline{i_0}$ must be kept to zero by choice of proper zero component of duty cycles and zero component, respectively. Normally a small ac component of the dc link voltages is accepted and the average of $\overline{i_0}$ during several switching periods is controlled to be zero.
- At low reference voltages a special situation is present. When $d_x=-d_z\le 1/2$ pulse pattern can be made symmetrical with regard to $d_0=\overline{\mu}_0=+1/2$ or $d_0=\overline{\mu}_0=-1/2$.

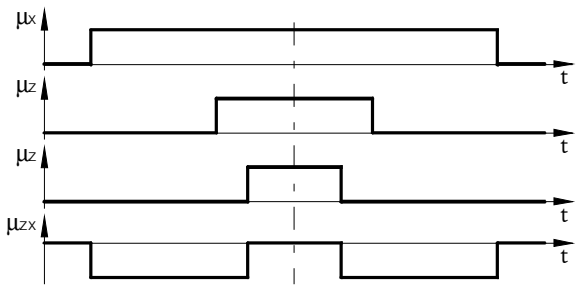

Fig. 8 Pulse pattern for low voltage level

If this possibility is used all voltages become either positive (for $d_x+d_z=1$) or negative (for $d_x+d_z=-1$) i.e. the switches of all phases make use of position 0 and + or 0 and -. Pulse pattern for $d_x+d_z=1$ is shown in Fig. 8 and for $d_x+d_z=-1$ in Fig. 9 respectively.
The sequence of steps given in this paper is not fixed and changes may be suitable depending on the conditions for practical implementation.

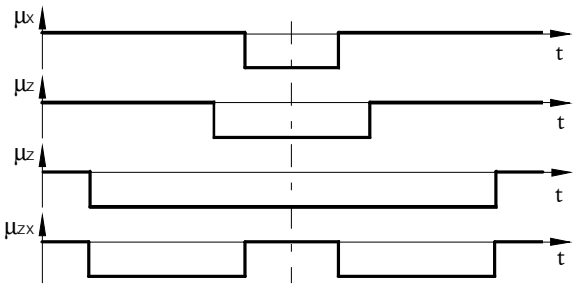

Fig. 9 Alternative Pulse pattern for low voltage level

5 Conclusion

Consideration of phase voltage delivers a clear insight into the physical processes of the converter. It can be used to perform so-called phase voltage modulation at which the handling of the zero component becomes very clear. The computational demand is the same as with vector modulation: Only few calculation is required and only few logical decisions have to be made. The modulation scheme can be used for rectifier and inverter applications and it can be adopted when switch positions '+' and '-' are realized by diodes only which can be the case at rectifiers.

References

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