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Prototype Drive and Modulation Concepts for DSP-Controlled Ultrasonic Motors powered by Resonant Converters

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Abstract. The driving principle of travelling wave ultrasonic motors (USM) is basically different from those of electromagnetic motors and requires thus tailored control schemes. This paper deals with newly developed analog and digital modulation concepts to drive a two-phase resonant converter, allowing a feeding of the USM with variable frequency, amplitudes and phase. A flexible experimental set-up for ultrasonic drives controlled by a DSP is presented including a suitable digital measuring system in order to realize efficiently control algorithms for the high level prototype drive.

Keywords. Ultrasonic Drives, Experimental Set-up, Frequency/Amplitude/Phase Modulation Concepts, Modulation Circuits, Measuring System

1 INTRODUCTION

Recently, USMs have attracted considerable attention as a new type of actuator in servo-systems. USMs combine features such as high driving torque at low rotational speed, high holding torque without an applied electric power, extremely low noise in operation, simple mechanical design and fast response.
In a travelling wave type USM two orthogonal vibration modes are excited to resonance by piezoelectric actuators. Due to the travelling wave the surface points of the stator perform an elliptic motion driving the rotor by frictional force, see [1],[2]. The electrical excitation of motor vibrations is applied by a two-phase inverter adding two series inductors and using the capacitance of the piezoceramics. Thus the motor becomes integral part of a resonant converter [3].
In practice, the inherent mechanical characteristic of USMs is widely nonlinear and time variant and change largely according to temperature effects due to operation conditions. Therefore the two-phase resonant converter feeding the USM must be driven by an adequate quantity of control parameters such as adjustable frequency, voltage amplitudes and phase difference to attain the best motor performance, especially in servo-system applications.
After an introduction about an experimental set-up for ultrasonic drives, the inherent typical characteristics of USM are outlined which yield to tailored driving circuits for the feeding two-phase resonant converter. The paper deals in detail with feasible analog and digital modulation concepts for a two-phase resonant converter in order to realize a flexible control scheme for a high level ultrasonic prototype drive controlled by a DSP. Finally, an appropriate digital measuring system for the phase and amplitude control of the drive is presented, extracting the fundamental fourier coefficients of the measured quantities by analog signal processing.

2 EXPERIMENTAL SET-UP FOR ULTRASONIC DRIVES

A flexible test set-up was realized with a structure given in Fig. 1 in order to investigate the characteristics of the USM, to verify the simulation model and to examine the control concepts by measurements. The digital control of the ultrasonic drive is performed for a prototype by a DSP-Board DS1003 (floating point). Interactive communication between the development software for the control and the DSP-Board is carried out via AT-BUS. The bidirectional data communication (regulating and measured quantities) between the DSP-Board and the system periphery (peripheral board no. 1 through 3) is obtained by the "Peripheral High Speed Bus" (PHS-BUS). The DSP-Board is modular extendable in order to realize the newly developed, specific peripheral electronic for the prototype drive.

The loading of the USM-drive is performed by a permanent magnet exited dc-machine with low rated speed and which owns a small ratio of inertia to rated torque. Initially it is operated current controlled but potentially it can be also speed controlled. Its range of operation is bound by a limitation of the current setting, depending on its direction, in a way that the ultrasonic drive operates stationary only as motor. Otherwise a high durability of the rotor contact layer cannot be guaranteed for the USM. The desired load torque can be adjusted by a proper setting of the armature current which can be performed either by the software via peripheral board no. 3 or alternatively by the analog setpoint adjuster. In the latter analog measuring instruments are integrated, allowing visual monitoring of speed and torque. A very accurate determination of the position and speed for the digital control is obtained by the evaluation of two sinusoidal tracksignals from the encoder by means of an ASIC (peripheral board no. 3), giving a maximal angle resolution of $360° / 2^{20} \cong 3{,}4 \cdot 10^{-4}\circ$.

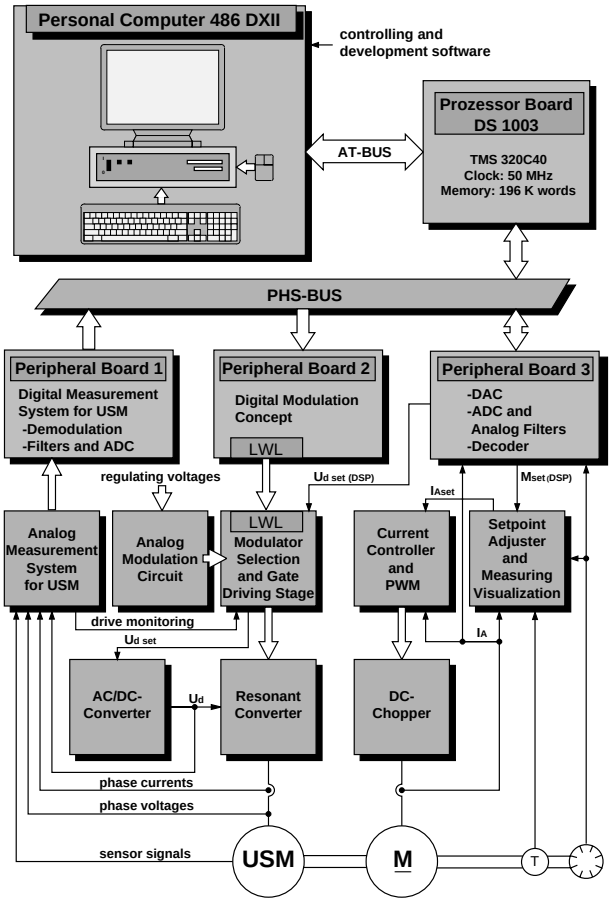

Figure 1: Experimental set-up for ultrasonic drives

The USM is powered by a two-phase resonant converter, which is supplied via an ac/dc-converter by a variable dc-link voltage. Two modulation circuits were developed for the operation of the resonant converter. The simple analog modulation circuit is applied for measurements like experimental examination of the small-signal behaviour. The newly developed digital modulation concept (peripheral board no. 2) serves as pulse-shaping block in the framework of the digital control scheme for the ultrasonic drive. The user selects the modulator, which includes as well some protective measures like over-current and over-voltage protection and a limitation of the maximum bending wave amplitude. Then the isolated gating signals are generated considering the necessary switch-on delay times.
Sensor signals detecting the two standing waves, phase currents and voltages are measured and passed to the digital measurement system (peripheral board no. 1). This extracts the real and the imaginary parts of the fundamental and transfers the digital information to the DSP for the control algorithm.

3 CHARACTERISTICS OF ULTRASONIC DRIVES

3.1 Characteristics of ultrasonic motors

Stationary models for the USM are required for the design of a resonant converter feeding the USM. In [1],[3] a simple equivalent circuit model is given, derived by electromechanical conversion theory of ultrasonic vibrating transducer systems. For the modelling approach a perfect symmetrical motor is assumed. Omitting thus the mechanical cross-couplings between both phases the mechanical behaviour of the motor with two phases can be replaced by two independent equivalent circuits, as given for one phase in Fig. 1. The bending wave of the sta-

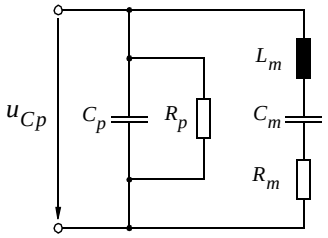

Figure 2: Equivalent circuit of USM

tor generated by the piezoceramic is characterized by the series resonance circuit consisting of L_m, C_m, R_m. Load conditions are modelled by variation of R_m. The capacitive behaviour of the piezoceramic is reflected by the parallel located capacitor C_P and the losses are considered by the parallel resistance R_P.
In order to evaluate the frequency control range the frequency response of the input admittance as depicted in Fig. 4 is considered. Only the descending section situated at the right side of the resonant peak is commonly used for the operation of the motor, since discontinuations occur below of the maximum, not modelled by the equivalent circuit, see [3]. Furthermore the marked narrow control range of about $300Hz$ is shifted in a large frequency range of several kHz by temperature effects during operation and requires thus a suitable frequency variation (high frequency resolution versus total operation range).

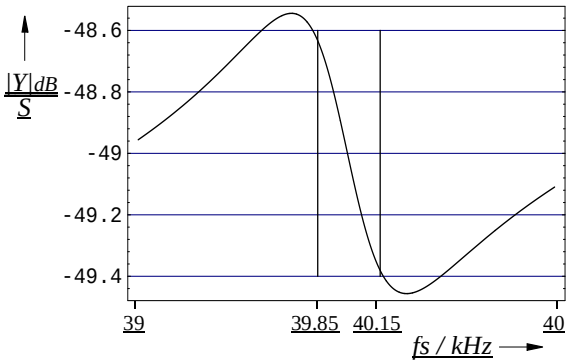

Figure 3: Admittance curve of network in Fig. 1

3.2 Selection of power electronic circuit

Since a voltage inverter is to be applied a series inductor has to be inserted between inverter and USM. Thorough inspection of inverter and motor results in the topology of a resonant converter, as given by Fig. 4 and Fig. 1. The series inductor is designed in a way that the loaded resonant tank behaves inductive, thus the motor current lags the motor voltage. Hence, the zero-voltage switching mode of the parallel loaded series resonant converter is obtained, whereby the switching losses of power MOSFETs are eliminated approximately (see [4], Fig. 8).
The two-phase resonant converter is driven (Fig. 5) by an adequate control circuit in order to realize the feeding of USM by an adjustable voltage amplitude, frequency and phase, which is in accordance with a

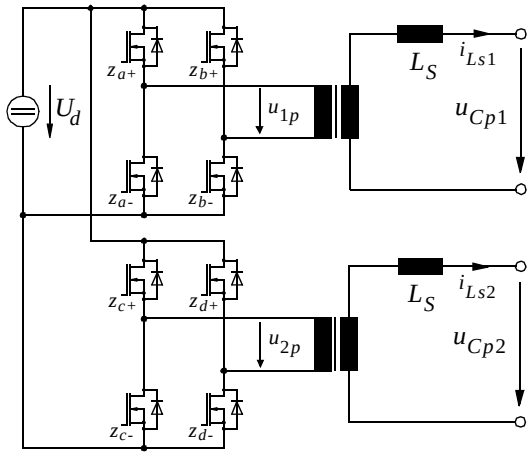

Figure 4: Two-phase resonant converter

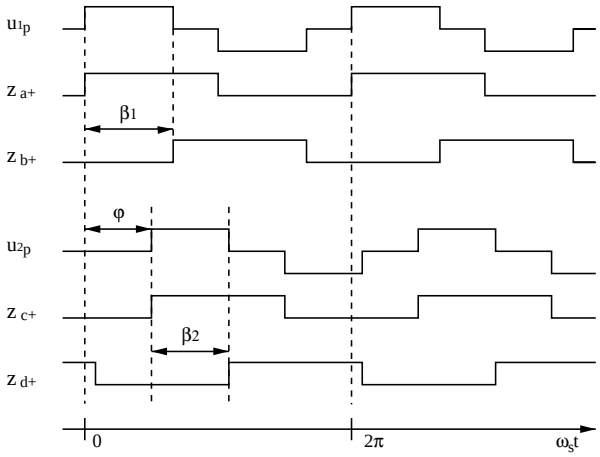

Figure 5: Inverter voltages in accordance with quantities f_S, φ, β_1, β_2

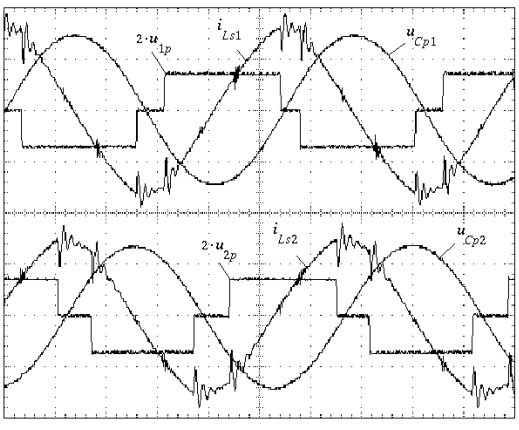

Figure 6: Measured voltages and currents of resonant converter

most flexible set-up for the USM controlling scheme. The voltage amplitudes are varied by the alteration of the dc-link voltage U_d of the inverter. A faster regulation of the respective voltage amplitudes results from the variation of phase shifts β_1, β_2, see Fig. 5, whereby even particular differing motor phase voltages can be used to compensate for manufacturing unsymmetries. The phase difference between phase voltages is denoted by φ which is to be adjusted at least in the range of $-90° \le \varphi \le 90°$ for speed reversals.

4 MODULATION CONCEPTS

The already cited control measures for the USM (electrical amplitude, switching frequency f_S and phase angle φ) influence the two vibration modes of the stator in order to vary the motor performance most flexibly due to the investigation phase, but imply considerable expenditures for the modulation circuit. Analog solutions as well as digital ones are described in the following and selected solutions have been evaluated.

4.1 Analog modulation circuit

A simple implementation for the required control concept is given in Fig. 10. The frequency adjustment is performed by a VCO depending on regulating voltage u_{fs}. The variation of phase angle φ with respect to the motor voltages is conducted by the cascaded modulators PWM1 and PWM2. Recent available phase shift controllers (PSC1, PSC2) are used to adjust the motor voltages u_{Cp1}, u_{Cp2}, whereby regulated quantities $u_{\beta 1}, u_{\beta 2}$ affect the phase shift between the driving signals of each inverter bridge. This results in a variable duty cycle of the bridge voltage, which equals the transformer primary voltage, Fig. 5. This analog modulation circuit suits especially well for analog control implementations.

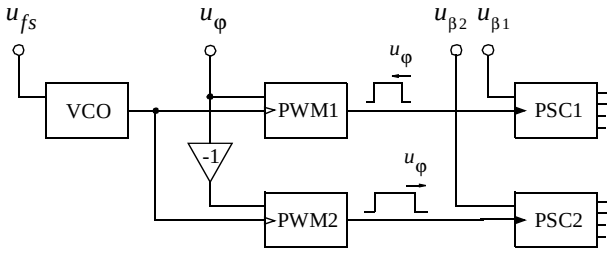

Figure 7: Analog control circuit for two-phase resonant converter

4.2 Digital modulation concept

Since a DSP is favoured for a most flexible control of the ultrasonic drive in the experimentation phase, a digital modulation concept is more suitable to generate the control waveform (Fig. 5) directly from the numerical data, calculated by a DSP. In addition to the latter, drifting of the point of operation affected by the temperature behaviour of the VCO can be avoided. This drifting leads to problems especially, if the drive is operated in an open-loop control due to the very narrow range of operation of the USM, see Fig. 4. Since the gain of the VCO is not known exactly due to temperature effects, the operating frequency is to be determined by measurements for the experimental set-up. Furthermore the response time of the analog modulator is not sufficient as to achieve a high dynamic. Thus, the development of a new modulation concept was motivated under the settings of a digital drive control.

First, the specifications for quantization of the regulating variables were laid down. For the control of piezoelectric motors on one hand a high frequency resolution due to the vary narrow frequency operation in the vicinity of the mechanical resonance (see. Fig. 4) is desired and on the other hand a large frequency range due to temperature effects caused by load conditions. Hence, for the digital modulation concept the following requirements were set:

- Switching frequency f_S: $30kHz \le f_s \le 50kHz$, $\Delta f_s < 1Hz$;
- Phase angle φ: $-180° < \varphi \le 180°$, $\Delta\varphi \le 1°$;
- Phase shift β_i: $0 < \beta_i \le 180°$, $\Delta\beta_i \le 1°$, $i = 1, 2$.

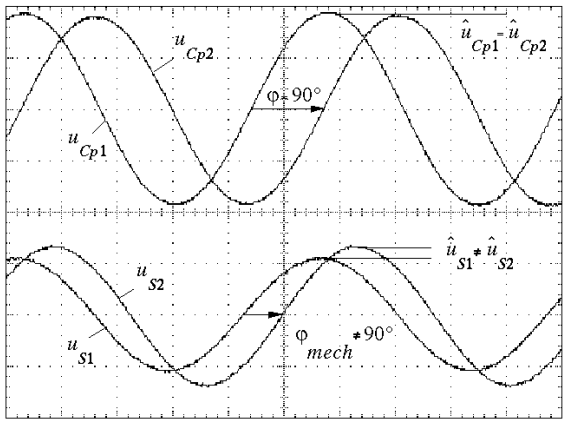

Figure 8: Measured phase voltages u_{Cp1}, u_{Cp2} and sensor signals u_{S1}, u_{S2} of USM in case of symmetrical feeding

As in the analog concept an independent adjustment of phase shift is feasible for both phases in order to compensate the unsymmetries of the motor phases verified by measurement in Fig. 8. The high flexibility of the control concept in conjunction with the full bridge topology is necessary to obtain an ideal travelling wave, which is not generally achieved in case of symmetrical feeding depicted in Fig. 8.

4.2.1 Basic concept. Essential building blocks of the digital modulator are a synthesizer and a dividing circuitry, see Fig. 10. A digitally setable frequency f_{clk} synchronized to the switching frequency of the resonant converter is derived by the synthesizer from a quarz stabilized system clock f_{sysclk}. In a second stage the four signals Q_A, Q_B, Q_C, Q_D with switching frequency f_S are generated by division, which are in accordance with the driving signals $z_{a+}, z_{b+}, z_{c+}, z_{d+}$ for the transistors given in Fig. 4 and Fig. 5. The phase angles between driving signals Q_B, Q_C, Q_D respective to Q_A are obtained by the programmable divider circuit, loaded with digital control words for $\varphi, \beta_1, \beta'_2$ with β'_2 equal to $\varphi + \beta_2$. The divisor of the frequency divider results from quantization specifications for $\varphi, \beta_1, \beta_2$. Since the angle resolution is supposed to be $1°$ the divider needs to divide by 360. Hence, the frequency f_{clk} results in $f_{clk} = 360\, f_S$ ($\Delta f_{clk} = 360\, \Delta f_S$), whereby the switching frequency range $30kHz \le f_s \le 50kHz$ is mapped in the frequency range $10{,}8MHz \le f_{clk} \le 18MHz$.

Ring counter circuits with a symmetrical output signal are qualified for the realization of frequency dividers. While f_{clk} is usually constant for the setting of the pulse-shaping block in case of PWM-inverters, an adjustable, digital synthesizer is required with a high frequency resolution in case of the ultrasonic drive to generate the variable f_{clk} due to the very narrow range of operation depicted in Fig. 4.

4.2.2 Frequency divider. A well known solution consists of digital counters with programmable ratio, producing the clocksignal f_{clk} by simply dividing the system clock f_{sysclk} following $f_{clk} = f_{sysclk}/N$. The required system clock results considering the resolution condition

$$\Delta f_{clk} = \frac{f_{sysclk}}{N} - \frac{f_{sysclk}}{N+1} = \frac{f_{sysclk}}{N(N+1)} \le \Delta f_{clkMAX} \qquad (1)$$

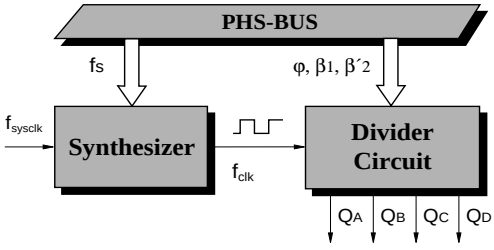

Figure 9: Basic concept for the digital modulator

for the total frequency range

$$f_{clkMIN} \le f_{clk} = \frac{f_{sysclk}}{N} \le f_{clkMAX}\,.$$

The condition is fulfilled, if $N_{MIN} = f_{sysclk}/f_{clkMAX}$ satisfies (1), yielding to the following inequality:

$$f_{sysclk} \ge \frac{f_{clkMAX}^2}{\Delta f_{clkMAX}} - f_{clkMAX} \qquad (2)$$

A frequency resolution of $\Delta f_{SMAX} = 1Hz$ ($\Delta f_{clkMAX} = 360Hz$) yields thus:

$$f_{sysclk} \ge \frac{(18MHz)^2}{360Hz} - 18MHz \cong 899{,}98GHz$$

Since there are no existing digital circuits operated at such high clock rates, the solution based on digital programmable dividers is seen to be impractical.

4.2.3 PLL. Instead the application of a PLL-synthesizer was investigated for a microprocessor based frequency modulation. In the field of telecommunications and electrical measuring PLL-synthesizers with a structure given in Fig. 10 are often applied for frequency synthesis, if signals with a high frequency stability are demanded.

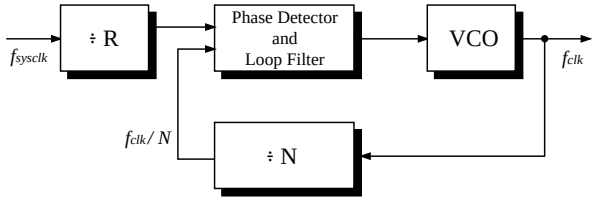

Figure 10: PLL-synthesizer

The output frequency of the circuit f_{clk} yields as fractional ratio of N to R as:

$$f_{clk} = N/R \cdot f_{sysclk} = N \cdot f'_{sysclk}\,, \text{ with } f'_{sysclk} = f_{sysclk}/R\,. \quad (3)$$

In order to obtain a fine frequency resolution versus a large range, $f'_{sysclkMIN} = f_{sysclk}/R_{MAX}$ results in a small quantity. But the quantity of $f'_{sysclkMIN}$ decides about the quality of the PLL-circuit, since the control bandwidth f_c of the phase control is set hereby.
Note, when designing the loop filter, that the control bandwidth f_c is displaced far enough from $f'_{sysclkMIN}$ in order to guaranty enough damping of f_{sysclk}. Otherwise the spectral purity descends extremely, if a modulation of the VCO with f_{sysclk} occurs [5].
Thus the dynamical behaviour of the phase control circuit is indirectly determined by f_{sysclk} via an accordingly fixed f_c. A high control bandwidth is the supposition for an oscillator with high stability and low settling time. Both features required for target application were not achieved by the synthesizer given in Fig. 10.

A fine frequency resolution with sufficient dynamic results using multiloop PLL-synthesizers. Due to the occurring frequency change moving spectral lines are generated, whereby the frequency distance to the carrier changes as the carrier frequency varies [5]. The spectral lines should be limited to a maximum amplitude to avoid negative effects. Practically the application of multiloop synthesizers means a (more or less good) compromise between the number of loops, with increasing costs and efforts, magnitude of reference frequencies and the magnitude of the respective spectral lines and is thus less suitable as solution.

Alternatively the method based on one-step fractional dividers was investigated resulting in adjustments with arbitrary fractional numbers. The known prescaler principle is applied, by which a predetermined time interval during a reference period is divided by ratio „a“ and the remaining time of the period is divided by „b“, see [5],[7]. In case of the „prescale principle“ two differing frequencies are compared to each other. This results in a non negligible ripple of the error signal of the phase detector reducing the spectral purity of the VCO-output. The detrimental modulation of the output signal is not to cure by an adequate higher damping factor of the loop filter, since the advantage of wide bandwidth f_c is lost. Thus, only the technically expensive solution remains to compensate the ripple of the error signal, since systematical disturbances are known prior.

4.2.4 DDS. The „Direct Digital Synthesizer“ (DDS) represents a recent method to generate the required output frequency from a digital control word. Its principle of operation is depicted in Fig. 10, see also [6],[7].

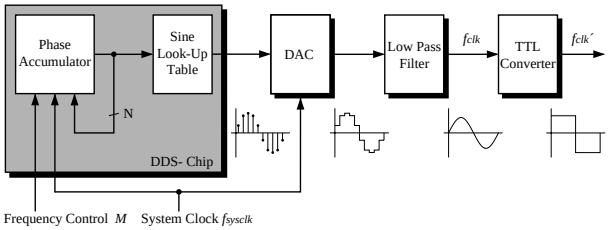

Figure 11: Direct Digital Synthesizer

In a phase accumulator with a width of N-bit the digital frequency control word which equals the phase increment M is added clock synchronously with f_{sysclk} to the actual phase value. The digital phase information serves as adress information for a lookup-table (LUT), containing the amplitude values of a sinusoidal signal for one period. Each phase value represents a certain value of the digital sinusoidal output signal of the LUT. The smallest adjustable frequency is generated, when the LSB of M is added to the accumulator which then increments all possible states, one at a time and synchronously controlled by f_{sysclk}. This will take 2^N clock cycles for an N-bit accumulator. Hence, the smallest digital phase information equals the frequency resolution of the DDS:

$$\Delta f_{clk} = \frac{f_{sysclk}}{2^N}\,. \qquad (4)$$

If an arbitrary phase increment M is added to the phase accumulator, the phase value is M-times larger than the LSB. Thus the frequency of the sinus signal results to

$$f_{clk} = M \cdot \frac{f_{sysclk}}{2^N} = M \cdot \Delta f_{clk}\,. \qquad (5)$$

According to Nyquist-theorem the maximum output frequency has to be adjusted smaller than half the system clock frequency $f_{clkMAX} \le f_{sysclk}/2$. Otherwise aliasing occurs. The producers of DDS recommend a maximum output frequency of 0,4 times f_{sysclk}, in order to suppress the first occurring alias frequency $f_{1Alias} = f_{sysclk} - f_{clk}$ by the low-pass filter sufficiently.

In addition the system cycle f_{sysclk} is determined by the maximum processing speed of the type of logic used. Trade offs for DDS are not only the limited bandwidth but also its smaller spectral purity as compared to state of the art PLL-circuits, affected by the limited resolution of the DAC. Since the amplitude quantization of the LUT-output is smaller than the phase quantization (N-bit) with respect to the limited resolution of the DAC a faulty approximation is transferred to the DAC first, minimizing the spectral purity. The following low-pass filter eliminates this fault largely. It is as well used to suppress the harmonics (alias frequencies) of the DDS explained above, occurring due to high output frequencies. That is the reason why the generation of the digital signal f'_{clk} is performed via a DAC, a low-pass filter and a backconversion into a digital signal using a TTL-converter. The obvious use of the MSB of the phase accumulator, indicating the positive or negative sign of the sinusoidal signal miscarries commonly according to the insufficient spectral purity, see [6].

The unique features of the DDS are very fine frequency steps, determined by the *N*-bit of the phase accumulator and nearly transient-free frequency changes. Since a new phase increment M can be applied to the phase accumulator after each cycle of f_{sysclk}, a very small settling time results, depending only on the speed of available logic.

Compared to the PLL-techniques the DDS-method proves to be the better solution for the required synthesizer of the digital control concept, because the high frequency resolution on one hand and on the other hand the fine dynamic qualities with respect to the drive control are the major demands. The disadvantage of less spectral purity is not as deciding as the latter properties, since the cascaded divider circuit causes short-time averaging, improving thus the spectral purity to an extend that is sufficient for this application.

4.2.5 Realization of the digital modulator. Under consideration of the previously fixed specifications ($\Delta\varphi = \Delta\beta_1 = \Delta\beta_2 = 1° \Rightarrow f_{clk} = 360\, f_S$) an according DDS-chip was selected with $N = 24$ and $f_{sysclk} = 50MHz$. With (4) a frequency resolution of $\Delta f_{clk} \cong 3Hz$ results. The squarewave output signal clocks the highly integrated divider circuit with divisor 360 for the generation of driving signals Q_A, Q_B, Q_C, Q_D according to angle $\varphi, \beta_1, \beta'_2$. Thus, a frequency resolution of switching frequency f_S yields of $\Delta f_S = \Delta f_{clk}/360 = 7{,}63mHz$, which satisfies the requirements easily. Noise effects can be suppressed, if the driving signals are connected to the test drive via fibres (LWL, see Fig. 1). The total concept of the digital modulator (peripheral board no. 2) was shown before in Fig. 10, indicating the transfer of newly calculated digital words for $f_S, \varphi, \beta_1, \beta'_2$ at the rising edge of Q_A.

4.2.6 Verification. The operation principle of the digital driving concept is demonstrated for a transient of the regulating quantities. For this case the outputs Q_A, Q_B, Q_C, Q_D, the difference signals $Q_A - Q_B$, $Q_C - Q_D$ which reflect the inverter output u_{1p}, u_{2p}, are depicted in Fig. 8.
With respect to the reference signal Q_A the difference signals do not contain a mean value, which of course is an absolute condition for the resonant converter as it contains a transformer. In the left half of Fig. 8 an adjustment was chosen similar to case a). Then a simultaneous variation of frequency and angle was adjusted by software according to case b) and transferred by the DSP to the modulator. The latter responds with a sudden alteration of the driving signals (right half of Fig. 8), assuming the new values with the next rising slope of Q_A centered in Fig. 8.
Thus, the digital modulator shows the anticipated dynamic behaviour for the drive control.

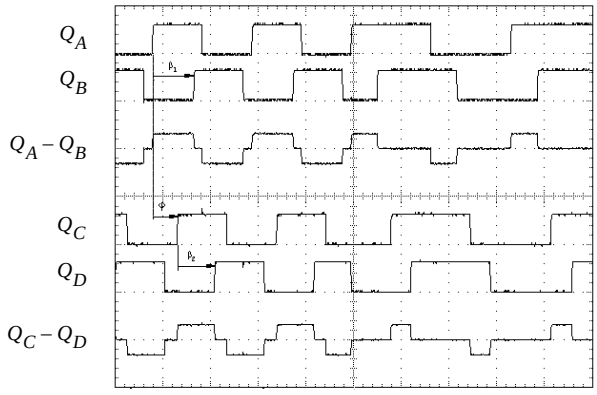

Figure 12: Measured output signals of digital modulator
case a): $f_S = 48kHz, \varphi = 90°, \beta_1 = 150°, \beta_2 = 135°$ (left half of Fig. 8)
case b): $f_S = 30kHz, \varphi = 90°, \beta_1 = 60°, \beta_2 = 45°$ (right half of Fig. 8)

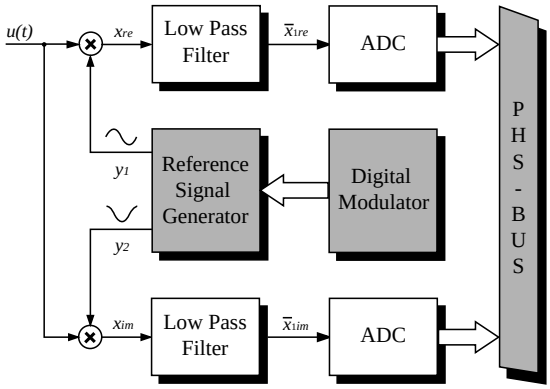

Figure 13: Measuring system by analog demodulation

5 DIGITAL MEASURING SYSTEM

The used power electronic circuit together with the inherent high switching frequency are not suitable for the control of instantaneous electrical quantities (like phase voltages or currents) and/or bending waves detected by sensor signals. Hence, amplitude and phase control concepts prove promising, only. For this reason, it is necessary to determine the fundamental quantities (amplitude and phase resp. real and imaginary part) of the fast varying measuring signals. A special signal processing circuit, yielding the fourier coefficients of the fundamental waveform offers the advantage, that the DSP-board is relieved of this task and can thus be utilized more efficiently for control tasks.

5.1 Signal processing by analog demodulation

For the extraction of the unknown fourier coefficients a method is applied originating from the telecommunication field and known as phase sensitive demodulation. The developed structure of the demodulator implemented in analog technique is shown in Fig. 10.
At the input of the demodulator a periodic measuring signal with a mean value of zero is applied, which can be described by the fourier series:

$$u(t) = \sum_{k=1}^{\infty} \hat{u}_k \sin(k\omega_S t + \varphi_k) \ .$$

This series is multiplied with a reference signal expressed by $y_1(t) = \hat{y}\sin(\omega_s t)$ in an analog multiplier. At its output the signal

$$x_{re}(t) = \hat{y}\sin(\omega_s t) \sum_{k=1}^{\infty} \hat{u}_k \sin(k\omega_S t + \varphi_k)$$

results. An averaged value $\bar{x}_{re}$ yields, when the signal is passed through a low-pass filter:

$$\bar{x}_{re} = \frac{1}{T}\int_0^T \hat{y}\sin(\omega_s t) \sum_{k=1}^{\infty} \hat{u}_k \sin(k\omega_S t + \varphi_k) dt \ .$$

This expression can be simplified under application of the orthogonal relation

$$\lim_{T\to\infty} \frac{1}{T}\int_0^T \sin(l\omega_s t)\sin(k\omega_s t + \varphi_k) dt = \begin{cases} 0 & \text{for } k \neq l \\ \frac{1}{2}\cos\varphi_k & \text{for } k = l \end{cases} \qquad (6)$$

respectively for the fundamental ($l = k = 1$) to

$$\bar{x}_{1re} = \frac{\hat{x}_1 \hat{y}}{2}\cos\varphi_1 \ . \qquad (7)$$

If the input signal $u(t)$ is multiplied with a second signal $y_2(t) = \hat{y}\cos(\omega_s t)$ with $y_1 \perp y_2$ an analogous calculation gives

$$\bar{x}_{1im} = \frac{\hat{x}_1 \hat{y}}{2} \sin\varphi_1 . \qquad (8)$$

x_{1re} and x_{1im} can be viewed as real and imaginary part of a complex signal, supplied to the DSP via ADC (see Fig. 10) as digital information. Thus, the demodulator extracts the fourier coefficients of the fundamental wave from the signal $u(t)$.
The magnitude and phase of the fundamental wave with respect to reference signals are determined by the DSP as

$$\hat{u}_1 = \frac{2}{\hat{y}} \sqrt{\bar{x}_{1re}^2 + \bar{x}_{1im}^2} , \quad \varphi_1 = \operatorname{atan}\left(\frac{\bar{x}_{1im}}{\bar{x}_{1re}}\right) . \qquad (9)$$

In the orthogonal relation (6) it was assumed, that the corner frequency of the low-pass filter approaches zero. But this is not anticipated, as the filtered signals $\bar{x}_{1re}$ and $\bar{x}_{1im}$ do not change with time, which is essential for the control system. Hence, for the selection of the corner frequency one has to compromise between a sufficient dynamic at the demodulator and to fulfil the orthogonal relation approximately.

5.2 Realization and verification

Since the switching frequency of the ultrasonic drive varies, the reference signals (y_1, y_2) are to be tuned accordingly. The obvious solution is to generate the reference signals from the reference output Q_A of the digital modulator. For this purpose two step functions with phase shift of 90° are generated by an analog multiplexer using the information of the digital modulator. From this signals the sinusoidal reference signals y_1 and y_2 are obtained by low-pass filtering.
To determine the fundamental fourier coefficients of all six measuring quantities of the test-drive depicted in Fig. 1 six structures following Fig. 10 are to realize (peripheral board no. 1). Reference signals y_1 and y_2 are applied to the respective inputs of the multipliers of each demodulator, to yield a definite relation of the measuring system.

The verification of the phase sensitive demodulator is illustrated by Fig. 14 for real operating conditions. The oscillogram displays all signals of the demodulator given in Fig. 10. As measuring signal $u(t)$ a sensor signal $u_S(t)$ was used, which was adjusted by φ in a way, that $u(t)$ and $y_1(t)$ are in phase. The output quantities $\bar{x}_{1re}(t)$ and $\bar{x}_{1im}(t)$ of the analog multipliers contain in addition to the dc-term an ac-term of frequency $2 \cdot \omega_S$, since two sinusoidal signals are multiplied, containing ω_S. Due to the above mentioned phase relation between $u(t)$ and $y_1(t)$ at the output of the low-pass filter the maximum positive real part of $x_{1re}(t)$ results and a signal, identical to zero for $\bar{x}_{1im}(t)$. The ac-quantity $(2 \cdot \omega_S)$ is largely eliminated.
Hence, this verification shows that the demodulator represents an appropriate signal processing means to extract the fundamental fourier coefficients.

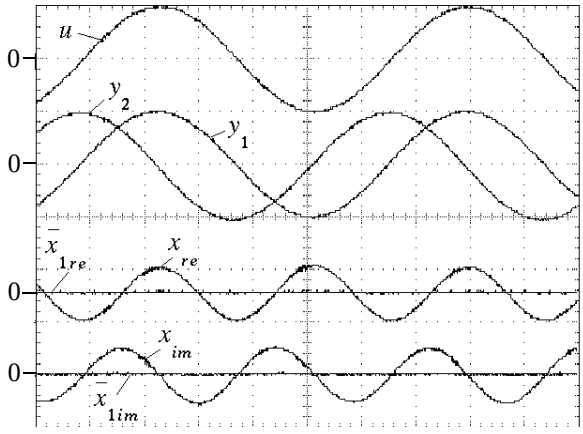

Figure 14: Measured signals of the analog demodulator

6. CONLCUSIONS

In this paper a flexible test set-up for the optimization of ultrasonic drives with high torque is illustrated followed by a brief summary of the motor characteristic which represent the base for the selection of the power electronic circuit. Two modulations concepts were derived, implemented and compared to alternatives in detail. The modulators in conjunction with the power electronic circuit allow an compensation of unsymmetries of the USM in order to obtain an ideal travelling wave.
Further investigations will center on the modelling of USM, the comparison of various control algorithms and the optimization of the overall system behaviour.

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