TITLE:

Design and Characterization of Basic Components for up to 160 Gbits/s Data Rate Communication Systems in 0.13 µm SiGe BiCMOS Technology

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ABSTRACT:

In recent years, the demand for analog bandwidth has increased manyfold for the communication, radar, and sensor applications. Inevitably, to meet the higher bandwidth demand, the analog components have to operate at increasingly higher frequency bands, which are opened up by state of the art semiconductor device technologies. However, while the domain of analog circuits has made continuous progress, the advancement in the digital circuits is much slower. Therefore, the purpose of this project is to push the maximum frequency of operation for in particular digital circuits. So basic building blocks of a digital 4:1 multiplexer (MUX) for data rates up to 160 Gbits/s, namely voltage-controlled oscillators (VCOs), frequency dividers, and phase-locked loops (PLLs) are intended to be designed and characterized in this project. One potential application can be seen in digital short range communication, e.g. chip-to-chip.

Colpitts and ring-type oscillators have been investigated for 160 GHz fundamental **VCO** design. A modified Colpitts topology has shown promising results and a VCO with tunable oscillating frequency from 150 to 158.7 GHz has been designed and characterized so far.

Both dynamic and static **frequency divider** topologies have been investigated. A novel digital dynamic divider (with a divide ratio two) working in the wide range from 100 to 166 GHz has been designed and characterized. A slightly modified conventional D- flip-flop based static frequency divider circuit (with a divide ratio two) has been successfully demonstrated as well. It works over the frequency range from DC up to 129 GHz.

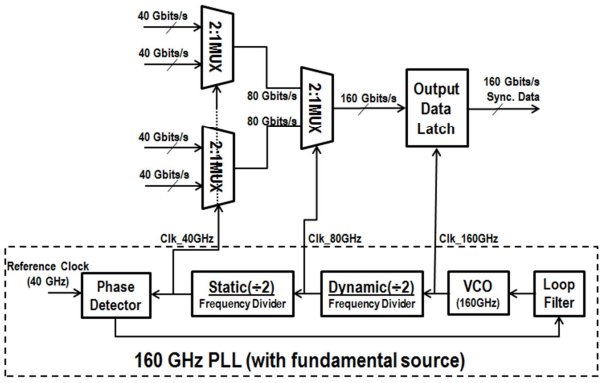

Fig. 1. The proposed 160 Gbits/s 4:1 MUX architecture

The successfully demonstrated VCO, dynamic frequency divider, and static frequency divider were integrated to form a **phase locked loop (PLL)** in the next phase. An initial experiment of 120 GHz PLL has been successfully demonstrated. In the next phase, the frequency of the PLL has to be raised further to enable its utility as a clock synthesizer circuit for up to 160 Gbits/s **4:1 multiplexer (MUX)**. The block diagram of the proposed 160 Gbits/s 4:1 MUX is shown in Fig. 1.